OKI semiconductor

MSM51C256

T-46-23-15

262,144 WORD X 1-BITS DYNAMIC RAM

GENERAL DESCRIPTION

The MSM51C256 is a new generation dynamic RAM organized as 262,144 words by 1 bit. The technology used to fabricate the MSM51C256 is OKI's CMOS silicon gate process technology. The device operates at a single + 5V power supply. Its I/O pins are TTL compatible.

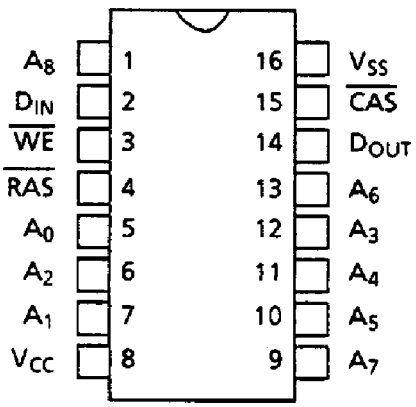
FEATURES

- Silicon gate, double polysilicon CMOS, 1-transistor memory cell
- 262,144 words by 1 bit
- Standard 16 lead plastic DIP/18 lead PLCC
- Family organization

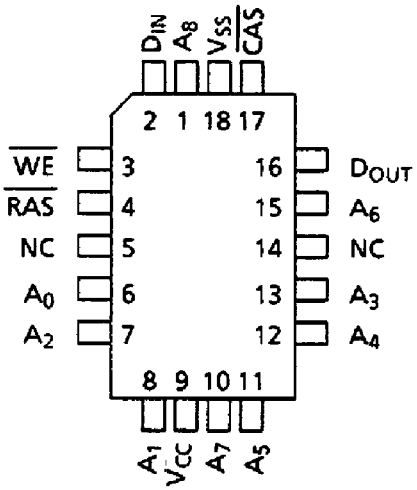
Family	Access Time (MAX)	Cycle Time (MIN)	Power Dissipation	
			Operating (MAX)	Standby (MAX)
MSM51C256-80	80 ns	160 ns	330 mW	20 mW
MSM51C256-10	100 ns	190 ns	275 mW	

- Single + 5V supply, ± 10% tolerance
- Input: TTL compatible, address input, data input latch
- Output: TTL compatible, tristate, nonlatch
- Refresh: 256 cycles/4 ms
- Common I/O capability using "Early Write" operation
- Fast page mode, read/write capability
- $\overline{CAS}$ before $\overline{RAS}$ refersh, Hidden refresh, RAS only refresh capability
- "Gated" $\overline{CAS}$
- Built-in V_{BB} generator circuit

MSM51C256RS
16 Lead Plastic DIP PIN CONFIGURATION
Top View



MSM51C256JS
18 Lead PLCC Package PIN CONFIGURATION
Top View



• DC Characteristics

(V_{CC} = 5V ± 10%, Ta = 0 to + 70°C)

Parameter	Symbol	Conditions		MSM51C256 -80		MSM51C256 -10		Unit	Note
				Min	Max	Min	Max		
Output high voltage	V_{OH}	I_{OH} = − 5.0mA		2.4	−	2.4	−	V	
Output low voltage	V_{OL}	I_{OL} = 4.2mA		−	0.4	−	0.4	V	
Input leakage current	I_{LI}	$V_{SS} \leqq VI \leqq V_{CC}$ all other pins not under test = 0V		− 10	10	− 10	10	μA	
Output leakage current	I_{LO}	D_{OUT} disable $V_{SS} \leqq VO \leqq V_{CC}$		− 10	10	− 10	10	μA	
Average power supply current* (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = min		−	60	−	50	mA	
Power supply current" (Standby)	I_{CC2}	$\overline{RAS} = V_{IH}$ $\overline{CAS} = V_{IH}$ D_{OUT} = Hz	TTL	−	3.5	−	3.5	mA	
			MOS	−	2.5	−	2.5	mA	
Average power supply current* ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ = cycling, $\overline{CAS} = V_{IH}$ t_{RC} = min		−	60	−	50	mA	
Average power supply current* ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ = cycling, $\overline{CAS}$ before $\overline{RAS}$		−	60	−	50	mA	
Average power supply current* (Fast page mode)	I_{CC7}	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ = cycling t_{PC} = min		−	40	−	35	mA	

*Note: I_{CC} is dependent on output loading and cycle. Specified values are obtained with the output open.

• Capacitance

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	TYP	MAX	Unit
Input capacitance (A0 to A8, D_{IN})	C_{IN1}	−	−	4	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	−	−	5	pF
Output capacitance (D_{OUT})	C_{OUT}	−	−	6	pF

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● AC Characteristics

(V_{CC} = 5V ± 10%, Ta = 0 to + 70°C) Note 1, 2, 3

Parameter	Symbol	MSM51C256 -80		MSM51C256 -10		Unit	Note
		Min	Max	Min	Max		
Refresh period	t_{REF}	–	4	–	4	ms	
Random read or write cycle time	t_{RC}	160	–	190	–	ns	
Read/write cycle time	t_{RWC}	185	–	220	–	ns	
Fast page mode cycle time	t_{PC}	55	–	55	–	ns	
Fast page mode read/write cycle time	t_{PRWC}	80	–	90	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	80	–	100	ns	4.5
Access time from $\overline{CAS}$	t_{CAC}	–	20	–	25	ns	4.5
Access time from column address	t_{AA}	–	40	–	50	ns	4.6
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	50	–	50	ns	4
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	–	0	–	ns	4
Output buffer turn-off delay	t_{OFF}	0	20	0	30	ns	
Transition time	t_T	3	50	3	50	ns	3
$\overline{RAS}$ precharge time	t_{RP}	70	–	80	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10K	100	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	20	–	25	–	ns	
$\overline{CAS}$ precharge time (Fast page mode cycle only)	t_{CP}	10	–	10	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10K	25	10K	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	–	100	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	60	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	50	ns	6
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	ns	
Row address set-up time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	12	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	20	–	ns	

• AC Characteristics (Cont.)

Parameter	Symbol	MSM51C256 -80		MSM51C256 -10		Unit	Note
		Min	Max	Min	Max		
Column address hold time from $\overline{RAS}$	t_{AR}	60	–	75	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	–	50	–	ns	
Read command set-up time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	8
Write command hold time from $\overline{RAS}$	t_{WCR}	60	–	75	–	ns	
Write command set-up time	t_{WCS}	0	–	0	–	ns	7
Write command hold time	t_{WCH}	15	–	20	–	ns	
Write command pulse width	t_{WP}	15	–	20	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	–	25	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	–	25	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	ns	
Data-in hold time	t_{DH}	15	–	20	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	60	–	75	–	ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	20	–	25	–	ns	7
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80	–	100	–	ns	7
Column address to $\overline{WE}$ delay time	t_{AWD}	40	–	50	–	ns	7
Read command hold time reference to $\overline{RAS}$	t_{RRH}	10	–	10	–	ns	8
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	30	–	30	–	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	10	–	10	–	ns	
$\overline{CAS}$ precharge time (Refresh counter test)	t_{CPT}	40	–	50	–	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	–	15	–	ns	

Notes: 1. An initial pause of 100 µs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.

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2. The AC characteristics assume at t_T = 5 ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2TTL + 100 pF.
5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
7. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if t_{CWD} (min.), $t_{RWD} \geqq t_{RWD}$ (min.) and $t_{AWD} \geqq t_{RWD}$ (min.) the cycle is read/write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

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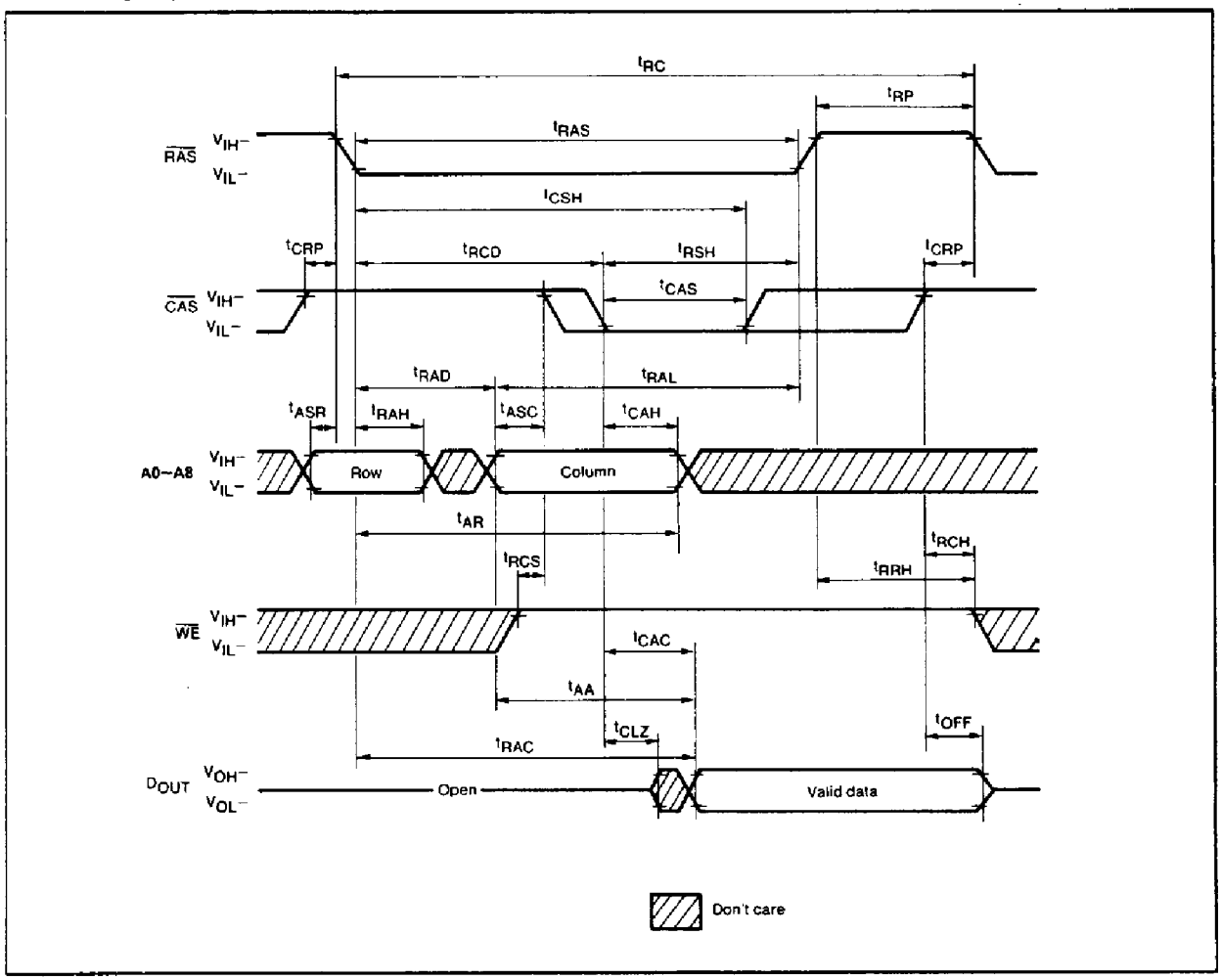
READ CYCLE



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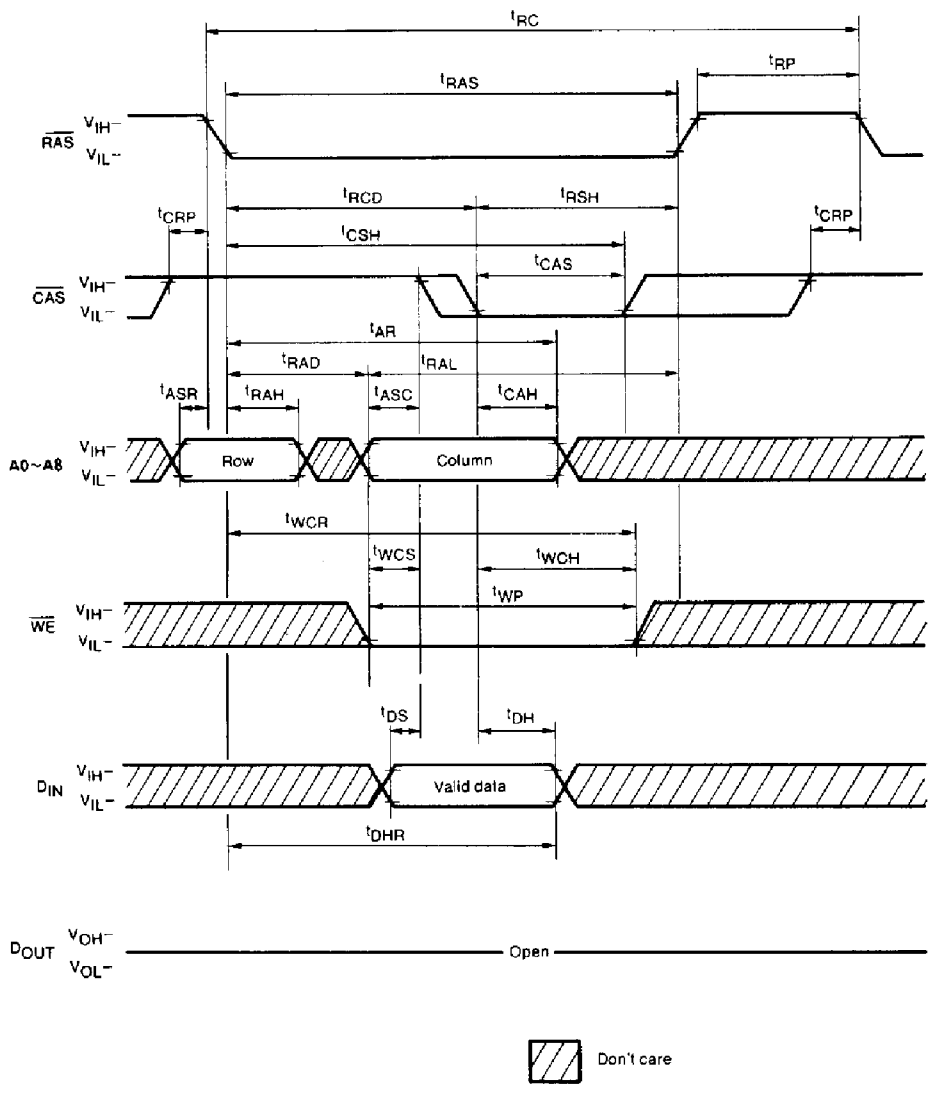
WRITE CYCLE (EARLY WRITE)



READ/WRITE CYCLE

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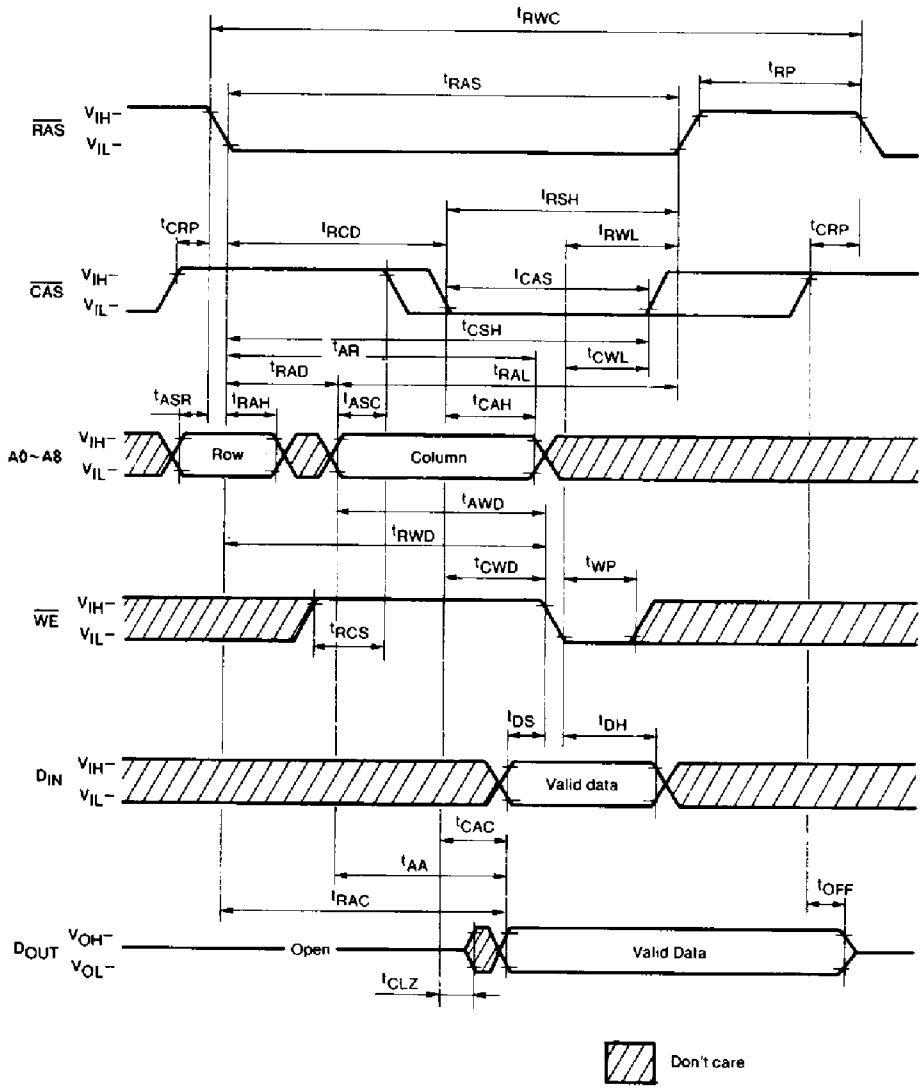

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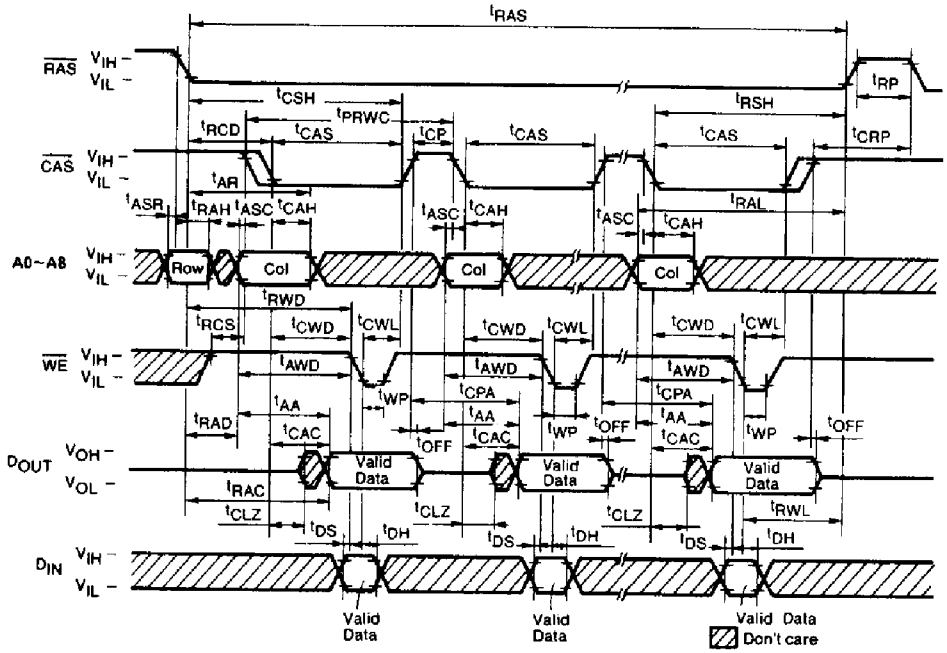
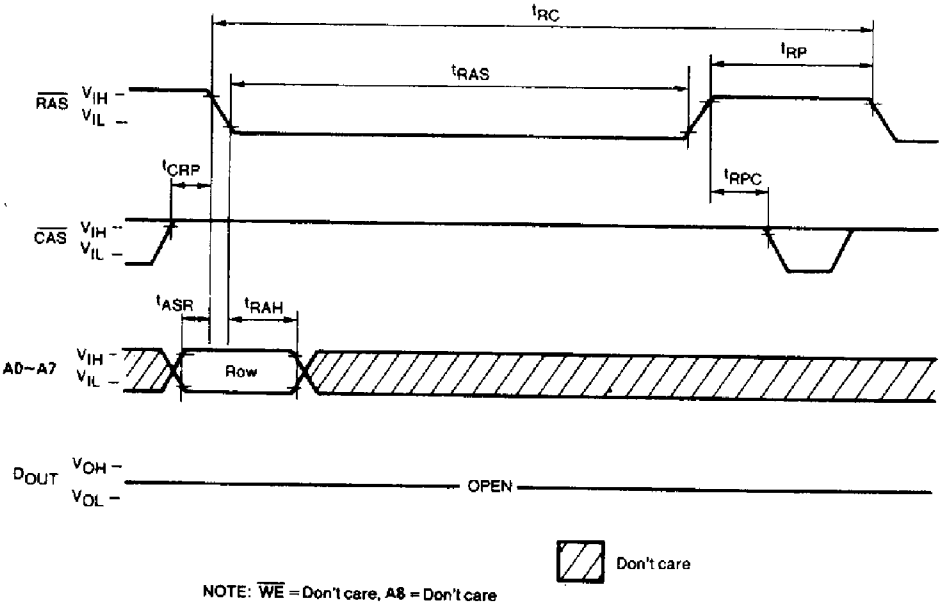
FAST PAGE MODE READ/WRITE CYCLE



RAS ONLY REFRESH CYCLE



NOTE: $\overline{WE}$ = Don't care, A8 = Don't care

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

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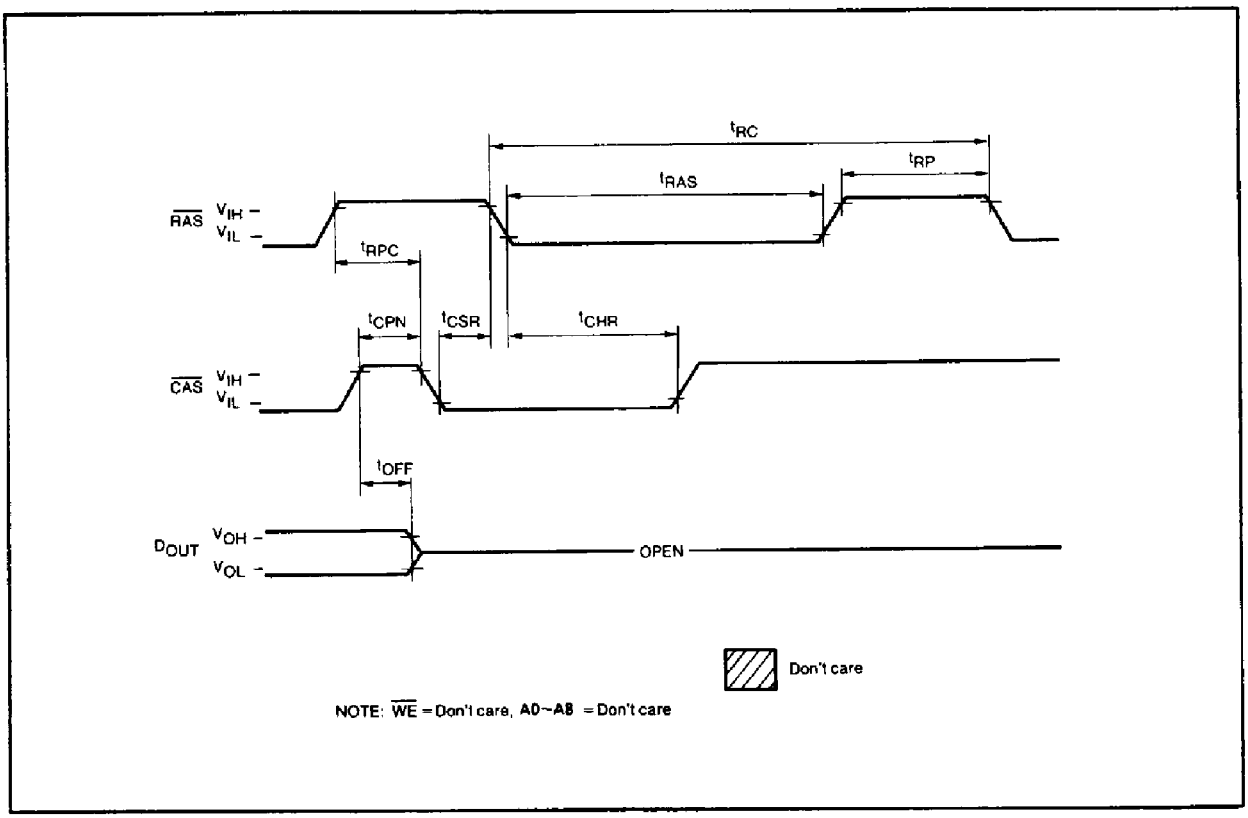

NOTE: $\overline{WE}$ = Don't care, A0~A8 = Don't care

FAST PAGE MODE READ CYCLE

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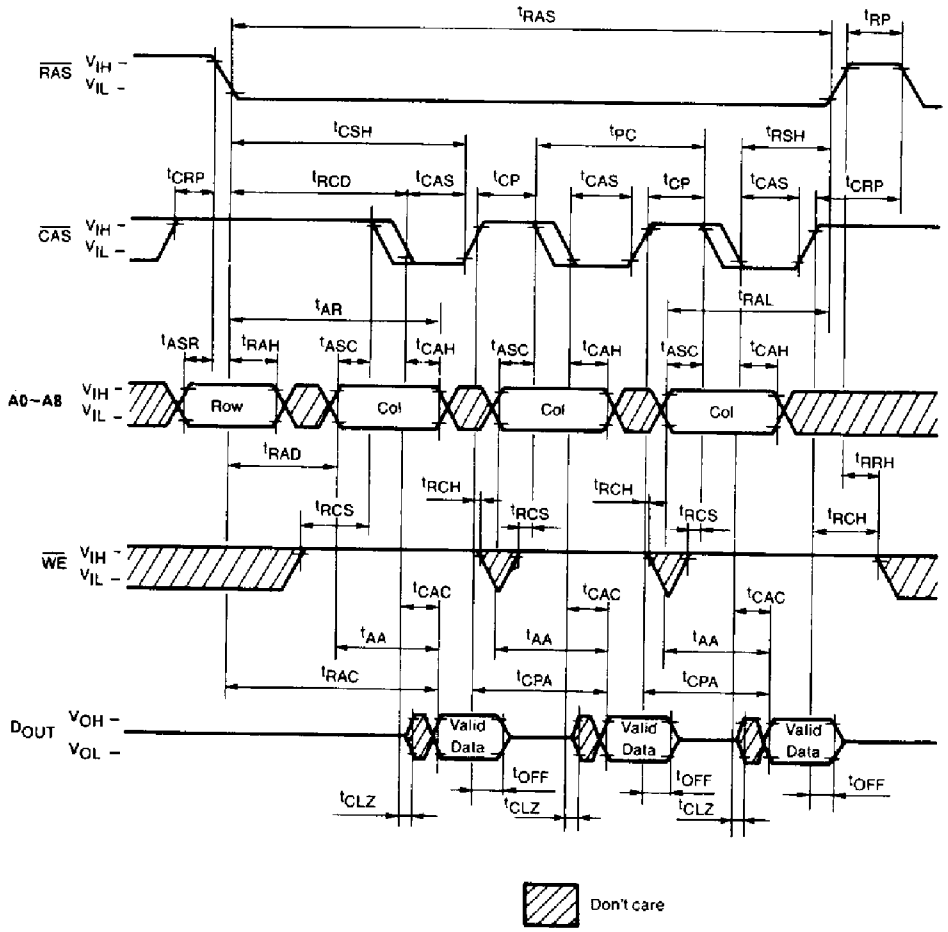

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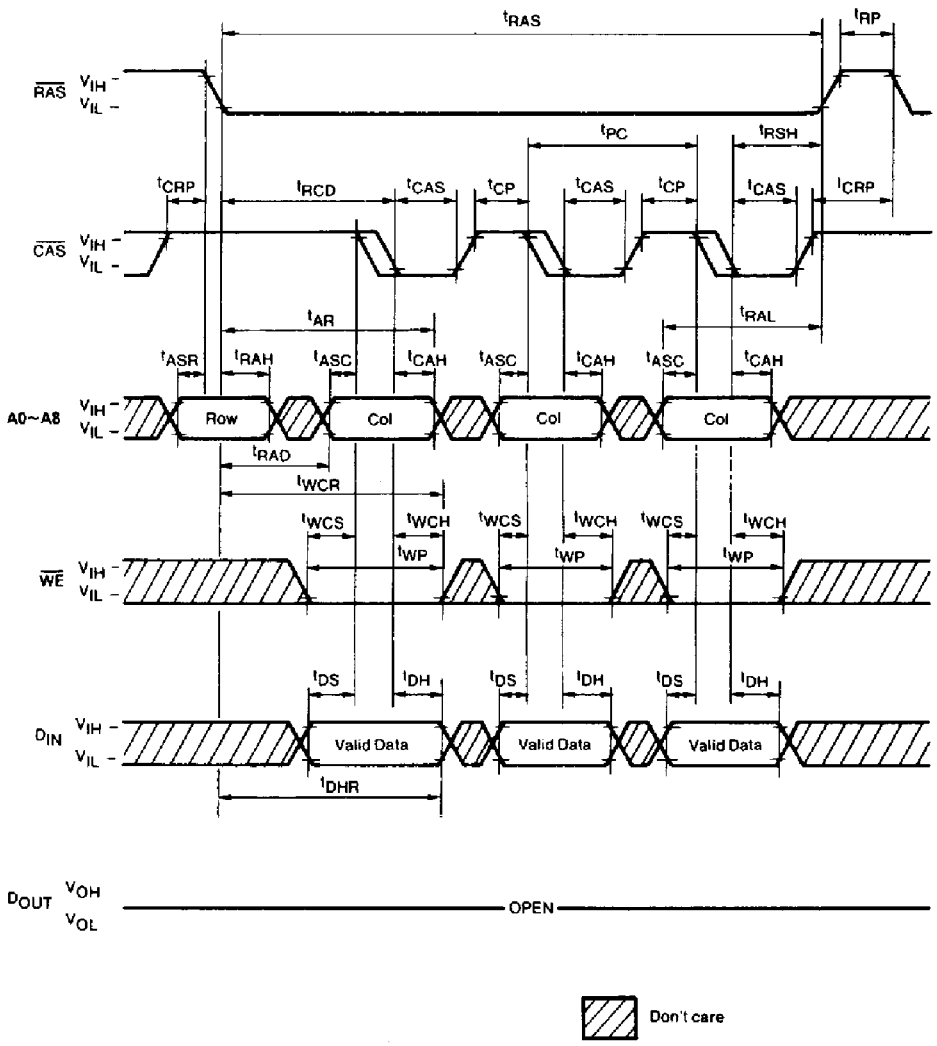
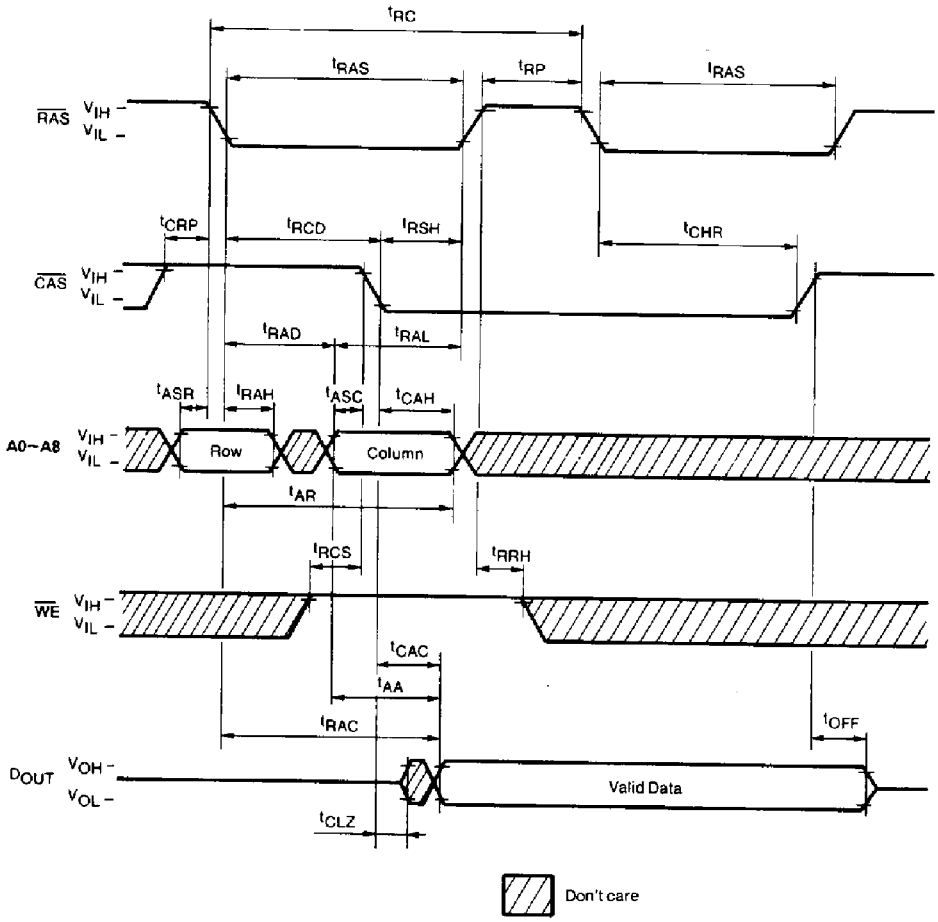
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE

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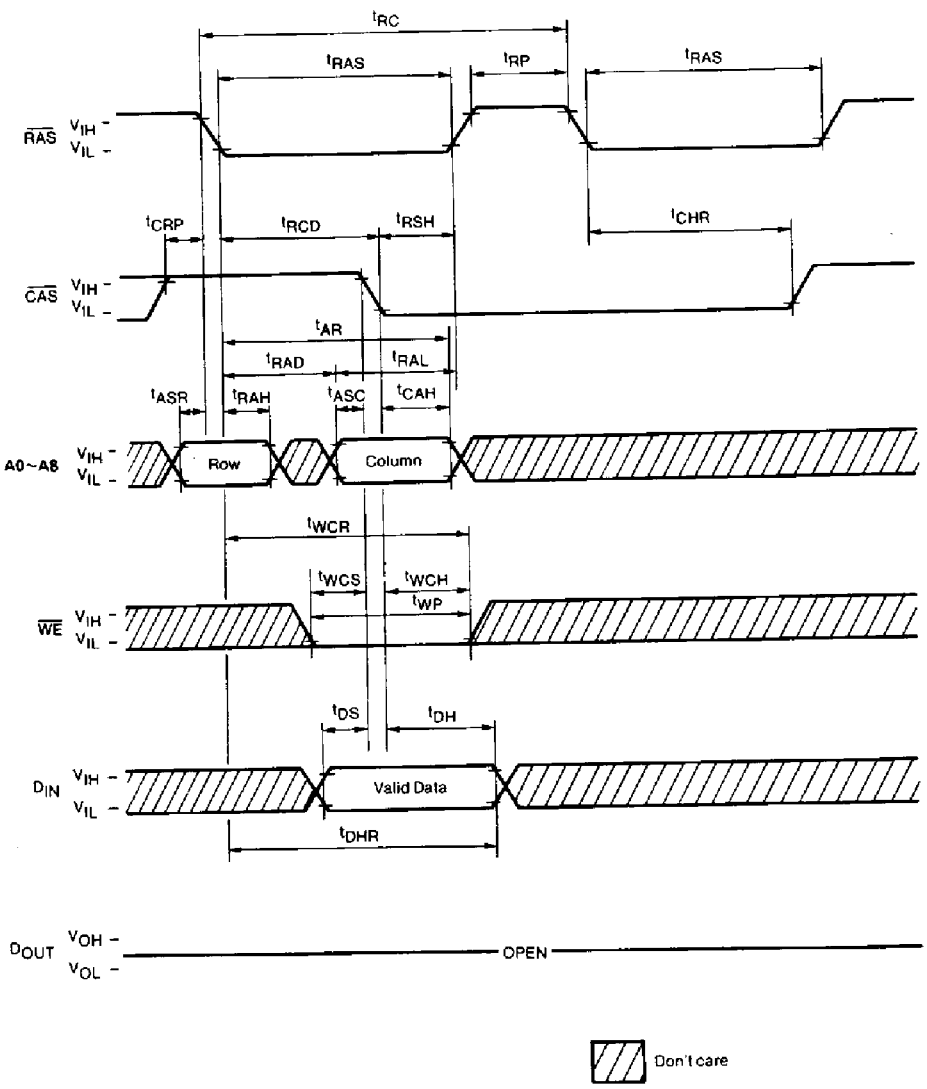

FUNCTIONAL DESCRIPTION

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Simple timing Requirements:

The MSM51C256 is a CMOS dynamic RAM optimized for high speed access time operations, low power applications. It is functionally similar to a traditional dynamic RAM. The MSM51C256 reads and writes data by multiplexing 18-bit address into 9-bit row and 9-bit column address. Because access time is primarily dependent on a valid column address rather than the precise time that $\overline{CAS}$ edge occurs, the delay time from $\overline{RAS}$ to $\overline{CAS}$ (t_{RCD}) has little effect on the access time. And the MSM51C256 can commit better memory system through-put during operations in an interleared system.

Fast-Read-While-Write Cycle:

The MSM51C256 has the fast read while write cycle which is achieved by excellent control of the three-state output buffer in adition to the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{WE}$ when $\overline{CAS}$ goes low. When $\overline{WE}$ is low during $\overline{CAS}$ transition to low, the MSM51C256 goes to early write mode where the output becomes floating and common I/O bus can be used on the system level. Whereas, when $\overline{WE}$ goes low after t_{CWD} following $\overline{CAS}$ transition to low, the MSM51C256 goes to delayed write mode where the output contains the data from the cell selected and the data from D_{IN} is written into the cell selected. Therefore, very fast read write cycle becomes available.

Address Inputs:

A total of eighteen binary input address bits are required to decode any 1 of 262,144 storage cell location within the MSM51C256. Nine row-address bits are established on the input pins (A_0 through A_8) and latched with the Row Address Strobe ($\overline{RAS}$). Then nine column adress bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$, $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Addres Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed form row-addresses to column-addreses.

Write Enable:

The read or write mode is selected with the $\overline{WE}$ input. A logic "high" on $\overline{WE}$ dictates read mode, logic "low" dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSM51C256 during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data in (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought "low" (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is storbed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until $\overline{CAS}$ is brought "low". In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max.). Data remain valid until $\overline{CAS}$ is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$ Only Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 to A_7) at least every 4 milliseconds. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of the 256 row-addresses (A_0 to A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$ only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh:

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the MSM51C256 offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh:

Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time from the previous memory read cycle. In MSM51C256 hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresha ddresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in this mode.