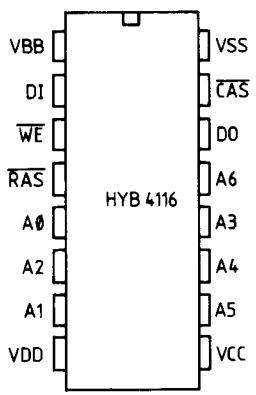
HYB 4116-2, HYB 4116-3
16,384-Bit Dynamic Random Access Memory (RAM)

- Fully decoded, 16,384 X1 bit organization
- Separate data input and output
- All inputs including clocks TTL compatible
- Low power dissipation
  462 mW active, 20 mW standby
  150 ns access time,
  320 ns cycle time (HYB 4116-P2)
  200 ns access time,
  375 ns cycle time (HYB 4116-P3)
- Three-state output, 2 TTL loads
- Compatible with MK 4116
- 128 refresh cycles
- Data output is unlatched

Pin Configuration



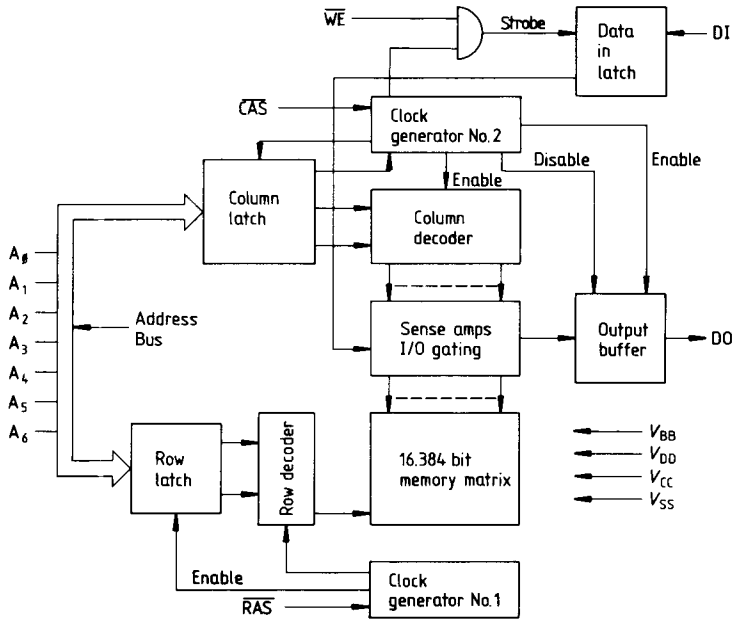
Pin Names

A0 – A6	Address inputs
CAS	Column address strobe
DI	Data in
DO	Data out
RAS	Row address strobe
WE	Read/write input
VBB	Power supply (−5 V)
VCC	Power supply (+5 V)
VDD	Power supply (+12 V)
VSS	Ground (0 V)

The HYB 4116 manufactured by Siemens is a dynamic random access memory built in N-channel silicon gate technology, using double layer polysilicon.

The dynamic one-transistor cell ensures high packing density and high speed. Moreover, multiplexing of the address signals permits the use of the space-saving 16-pin dual in-line package.

Block Diagram



Functional Description

Addressing (A0–A6)

For selecting one of the 16,384 memory cells, a total of 14 address bits is required which is consecutively applied via pins A0 to A6 by means of two strobes (address multiplexing). First the seven row addresses are called up and accepted with strobe $\overline{RAS}$ into the row select buffer. Following this, the seven column addresses are deposited in the column select buffer with $\overline{CAS}$. It should be noted that the address signals are available in their steady-state condition at the time of the negative pulse edge of $\overline{RAS}$ and $\overline{CAS}$, respectively.
$\overline{RAS}$ and $\overline{CAS}$ determine the starting point of the internal clock control.
$\overline{RAS}$ initiates row decoding and activates the read amplifier. $\overline{CAS}$ controls column decoding as well as the data input and output amplifiers.

Read write ($\overline{WE}$)

Read and write operations are executed when the write enable signal $\overline{WE}$ is at "H" or "L". Data input DI is disabled as long as reading takes place.
The shortest write cycle time is obtained when $\overline{WE}$ goes to logic "L" ahead of or simultaneously with $\overline{CAS}$ ("early write"). The write data is then accepted into the input data memory by means of $\overline{CAS}$.

Delayed writing, read-modify-write

If writing or read-modify-write is delayed, $\overline{CAS}$ is already at logic "L" so that the write data is transferred to the input data memory with the subsequent $\overline{WE}$ signal.

Data input (DI)

Data can be input during a write or a read-modify-write cycle. The strobe for the data input is the last one of signals $\overline{WE}$ or $\overline{CAS}$ to make its negative transition.

Data output (DO)

The data output may assume three states (Tri-state logic) and is rated for driving two TTL loads. As against the output data the input data is not inverted.
In a read cycle the read data is available after access time *t*CAC referred to $\overline{CAS}$. At the end of the read cycle, when $\overline{CAS}$ is again "H", the data output assumes again the high impedance condition.
In the case of read-modify-write the data output contains the data read from the selected cell as in the read cycle. For "early write" the output pin assumes a high impedance troughout the entire cycle.

Refresh cycle

To prevent data in the dynamic memory cells from getting lost, each row address must be called up at least every two milliseconds. A total of 128 refresh cycles must be executed for all row addresses during this 2 millisecond period.
During writing or reading the data in the 128 memory cells of a row-line is automatically refreshed.

Precharge cycle

After power is applied to the device, the HYB 4116 requires several cycles before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

Absolute Maximum Ratings *)

Operating Temperature Range	0 to 70 °C
Storage Temperature Range	−65 to 150 °C
Voltage on any pin relative to V_{BB}	−0.5 to 20 V
Voltage on V_{DD}, V_{CC} supplies relative to V_{SS}	−1 to 15 V
$V_{BB} - V_{SS}$ ($V_{DD} - V_{SS} \geq 0$ V)	0 V
Power Dissipation	1 W

D.C. Characteristics [1]

T_A = 0 to 70 °C; V_{SS} = 0 V, V_{DD} = +12 V ±10%, V_{BB} = −5 V ±10%, V_{CC} = +5 V ±10%

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
V_{IH}	High level input voltage, (all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$) [2]	2.4	7.0	V	–
V_{IHC}	High level input voltage ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$) [2]	2.4	7.0		
V_{IL}	Low level input voltage [2]	−1.0	0.8		
V_{OH}	Output high voltage	2.4	V_{CC}		I_O = −5 mA
V_{OL}	Output low voltage	–	0.4		I_O = 4.2 mA
I_{DD1}	Average V_{DD} supply current [3]	–	35	mA	–
I_{DD2}	Standby V_{DD} supply current	–	1.5		$\overline{RAS}$ at V_{IH} $\overline{CAS}$ at V_{IH}
I_{DD3}	Average V_{DD} current during refresh [3]	–	27		$\overline{RAS}$ cycling $\overline{CAS}$ at V_{IH}
$I_{I(L)}$	Input leakage current (any input) [4]	−10	10	µA	–
$I_{O(L)}$	Output leakage current	−10	10		$\overline{CAS}$ at V_{IH} V_O = V_{SS} to V_{CC}
I_{CC}	V_{CC} supply current [5]	−10	10		$\overline{CAS}$ at V_{IH} $\overline{RAS}$ at V_{IH}
I_{BB1}	Average V_{BB} power supply current	–	200		–
I_{BB2}	Standby V_{BB} power supply current	–	100		

*) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
C_{I1}	Input capacitance [6] (A_0–A_6), DI	–	5	pF	–
C_{I2}	Input capacitance [6] $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	–	10		
C_O	Output capacitance [6]	–	7		DO disabled

1) The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC} and V_{SS} should never be 0.3 V more negative than V_{BB}.
2) Over- and undershooting on input levels of 6.5 V or −2 V for a period of 30 ns will not influence function and reliability of the device.
3) I_{DD} depends on frequency of operation. Maximum current is measured at the fastest cycle rate.
4) All device pins at 0 V except V_{BB} at −5 V and pin under test which is at +7 V.
5) V_{CC} is connected to output buffer only.
6) Effective capacitance calculated from the equation
$C = \frac{I \cdot \Delta t}{\Delta V}$ with $\Delta V = 3$ V.

A.C. Characteristics [1]

T_A = 0 to +70 °C; V_{SS} = 0V; V_{DD} = 12V ±10%; V_{BB} = −5V ±10%; V_{CC} = +5V ±10%

Symbol	Parameter	Limit Values				Units
		HYB 4116-P2		HYB 4116-P3		
		Min.	Max.	Min.	Max.	
t_{RC}	Random read or write cycle time [2]	320	–	375	–	ns
t_{RWC}	Read/write cycle time [2]	320	–	375	–	
t_{RMWC}	Read/modify/write cycle time [2]	320	–	405	–	
t_{RAC}	Access time from $\overline{RAS}$ [3] [4]	–	150	–	200	
t_{CAC}	Access time from $\overline{CAS}$ [3] [5]	–	100	–	135	
t_{OFF}	Output buffer turn-off delay [6]	–	40	0	50	
t_{RP}	$\overline{RAS}$ precharge time	100	–	120	–	
t_{RAS}	$\overline{RAS}$ pulse width	150	10^4	200	10^4	
t_{RSH}	$\overline{RAS}$ hold time	100	–	135	–	
t_{CSH}	$\overline{CAS}$ hold time	150	–	200	–	
t_{CAS}	$\overline{CAS}$ pulse width	100	–	135	–	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time [7]	20	50	25	65	
t_{ASR}	Row address set-up time	0	–	0	–	
t_{RAH}	Row address hold time	20	–	25	–	
t_{ASC}	Column address set-up time	−5	–	−10	–	
t_{CAH}	Column address hold time	45	–	55	–	
t_{AR}	Column address hold time referenced to $\overline{RAS}$	95	–	120	–	
t_T	Transition time (rise and fall)	3	35	3	50	
t_{RCS}	Read command set-up time (RMW)	0	–	0	–	
t_{RCH}	Read command hold time	0	–	0	–	
t_{WCH}	Write command hold time	45	–	55	–	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	95	–	120	–	
t_{WCS}	Write command set-up time [8]	−20	–	−20	–	

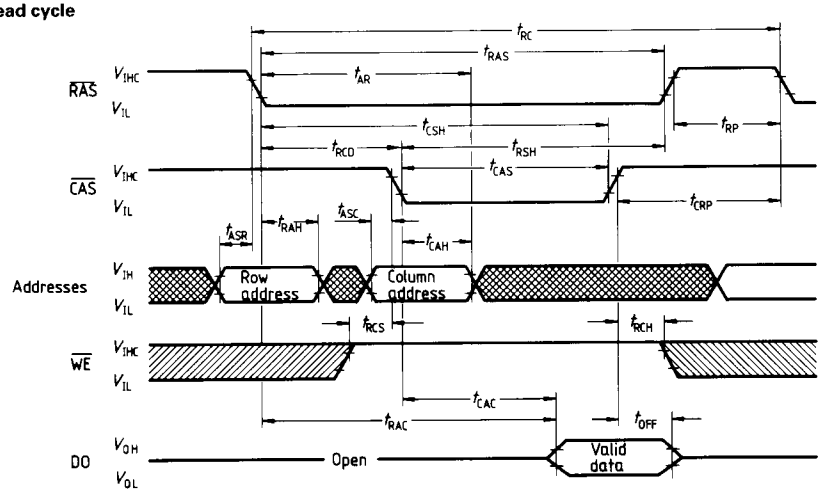
Symbol	Parameter	Limit Values				Units
		HYB 4116-P2		HYB 4116-P3		
		Min.	Max.	Min.	Max.	
t_{WP}	Write command pulse width	45	–	55	–	ns
t_{RWL}	Write command to $\overline{RAS}$ lead time	50	–	70	–	
t_{CWL}	Write command to $\overline{CAS}$ lead time	50	–	70	–	
t_{DS}	Data in set-up time	0	–	0	–	
t_{DH}	Data in hold time [9]	45	–	55	–	
t_{DHR}	Data in hold time [9] referenced to $\overline{RAS}$	95	–	120	–	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	−20	–	−20	–	
t_{RF}	Refresh period	–	2.0	–	2.0	ms
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ delay [8]	60	–	95	–	ns
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ delay [8]	110	–	160	–	

Notes:

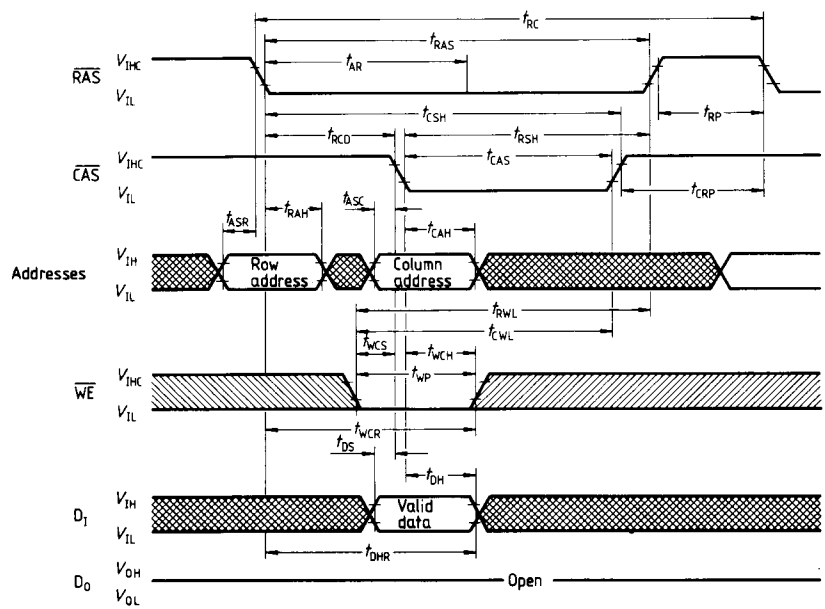
1) $V_{IHC\,(min)}$ or $V_{IH\,(min)}$ and $V_{IL\,(min)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
2) The specifications for $t_{RC\,(min)}$ and $t_{RWC\,(min)}$ are used only to indicate cycle time at which proper operation over full temperature range (0 °C ≤ T_A ≤ 70 °C) is assured.
3) Measured with a load equivalent to two TTL loads and 100 pF.
4) Assumes that $t_{RCD} \leq t_{RCD\,(max)}$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5) Assumes that $t_{RCD} \geq t_{RCD\,(max)}$.
6) $t_{OFF\,(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7) Operation within the $t_{RCD\,(max)}$ limit ensures that $t_{RAC\,(max)}$ can be met. $t_{RCD\,(max)}$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD\,(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
8) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geq t_{CWS\,(min)}$, the cycle is an early write cycle and the data-out pin will remain open circuit (high impedance) throughout the entire cycle: if $t_{CWD} \geq t_{CWD\,(min)}$ and $t_{RWD} \geq t_{RWD\,(min)}$ the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
9) t_{DS} and t_{DH} are referenced to the leading edge of $\overline{CAS}$ in early write cycles, and to the leading edge of $\overline{WE}$ in delayed write or read-modify-write cycles.

Waveforms

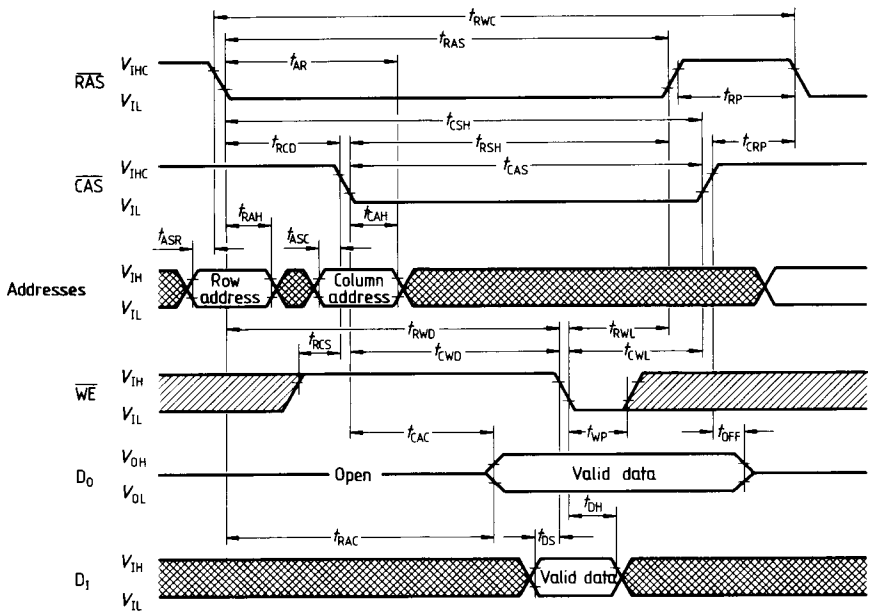
Read cycle



Write cycle (early write)

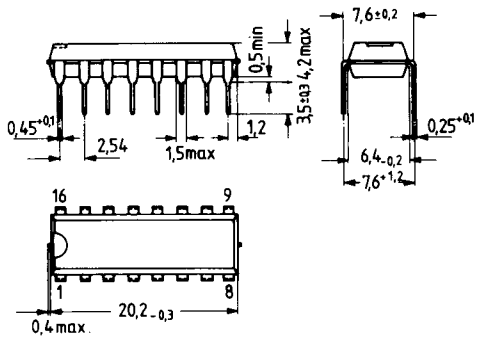


Read-write/read-modify-write cycle



Package Outline

16 Pin Plastic Package Type P



Ordering Information

Type	Description	Ordering Code
HYB 4116-P 2	RAM (Plastic; 150 ns)	Q67100-Q308
HYB 4116-P 3	RAM (Plastic; 200 ns)	Q67100-Q306