VL82C204

PC/AT-COMPATIBLE DATA BUFFER

FEATURES

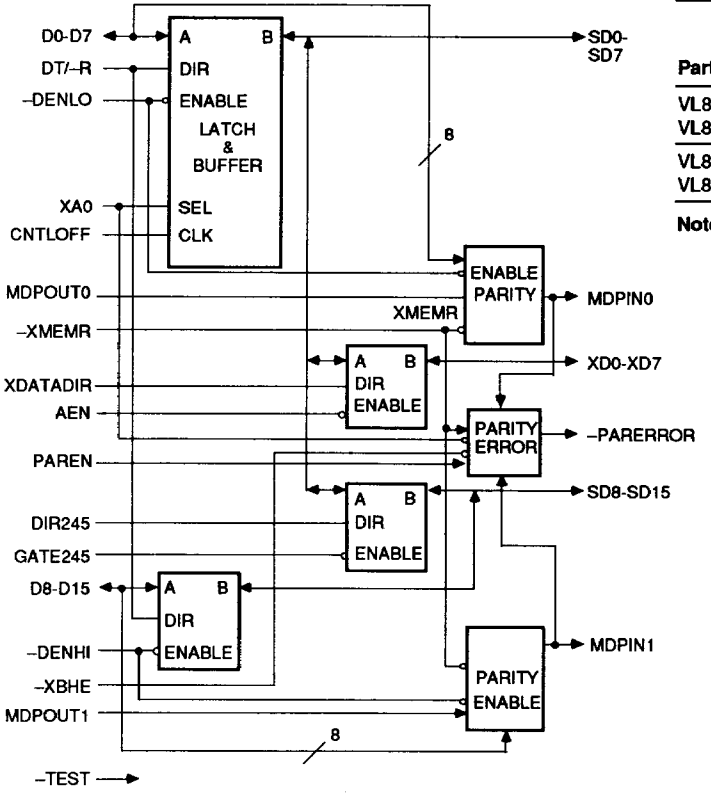
- Fully compatible with IBM PC/AT-type designs
- Completely performs data buffer function in IBM PC/AT-compatible systems
- Replaces several buffers, latches and other logic devices
- Supports up to 20 MHz system clock
- Device is available as "cores" for user-specific designs
- Designed in CMOS for low power consumption

DESCRIPTION

The VL82C204 PC/AT-Compatible Data Buffer provides a 16-bit CPU data bus I/O as well as 24 buffered drivers. The buffered drivers consist of 16 bidirectional system data bus drivers, each capable of sinking 24 mA (60 'LS loads) of current; eight bidirectional peripheral bus drivers, each capable of sinking 8 mA (20 'LS loads) of current. The VL82C204 also generates the parity error signal for the system.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in a JEDEC-standard 68-pin plastic leaded chip carrier (PLCC) package. The VL82C204 is part of the PC/AT-compatible chip sets available from VLSI. Please refer to the Selector Guide in the front of this manual.

BLOCK DIAGRAM



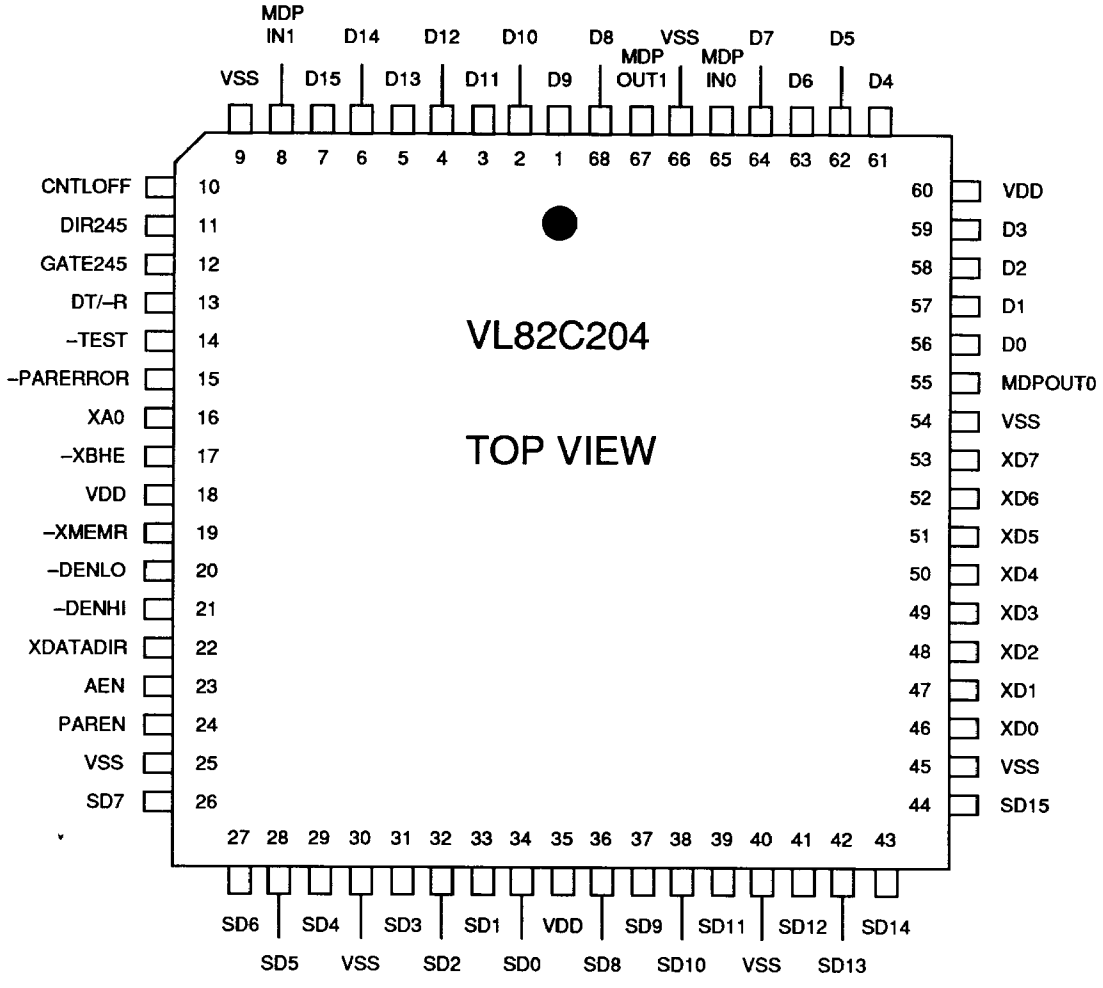
ORDER INFORMATION

Part Number	System Clock Freq.	Package
VL82C204-16QC VL82C204-16QI	16 MHz	Plastic Leaded Chip Carrier (PLCC)
VL82C204-20QC VL82C204-20QI	20 MHz	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range:
QC = 0°C to +70°C
QI = –40°C to +85°C.

4

PIN DIAGRAM


VL82C204
TOP VIEW
1 MDP IN1
2 D14
3 D12
4 D10
5 D8
6 VSS
7 D7
8 D5
9 VSS
10 D15
11 D13
12 D11
13 D9
14 MDP OUT1
15 MDP IN0
16 D6
17 D4
18 CNTLOFF
19 DIR245
20 GATE245
21 DT/-R
22 -TEST
23 -PARERROR
24 XA0
25 -XBHE
26 VDD
27 -XMEMR
28 -DENLO
29 -DENHI
30 XDATADIR
31 AEN
32 PAREN
33 VSS
34 SD7
35 SD6
36 SD5
37 SD4
38 VSS
39 SD3
40 SD2
41 SD1
42 SD0
43 VDD
44 SD8
45 SD9
46 SD10
47 SD11
48 VSS
49 SD12
50 SD13
51 SD14
52 SD15
53 VSS
54 MDPOUT0
55 XD0
56 XD1
57 XD2
58 XD3
59 XD4
60 XD5
61 XD6
62 XD7
63 VSS
64 D0
65 D1
66 D2
67 D3
68 VDD

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
CNTLOFF	10	I	This input is used as a clock to latch the current data on the low byte of the system or peripheral data bus. Data is latched and output to D0-D7 on the rising edge of CNTLOFF and is independent of the status of DT/–R, XA0, or –DENLO.
DT/–R	13	I	Data Transmit (high)/Receive (low) - This input is a signal from the bus controller. It establishes the direction of data flow to or from the system data bus.
–TEST	14	I	Test - This is an active low input which is used to three-state all outputs of the VL82C204 device. This is for system level test where it is necessary to overdrive the outputs of the VL82C204. When –TEST is low, all outputs and bidirectional pins of the VL82C204 will be three-stated. This pin should be pulled up via a 10K Ω pull-up resistor in a standard system configuration.
–DENLO	20	I	Data Enable Low - An active low input that enables a low byte data transfer on the CPU data bus low byte transceiver. When –DENLO is inactive, low byte parity is disabled.
XA0	16	I	Peripheral Address Bus Bit 0 - This is the LSB of the peripheral address bus. The signal is used throughout the system to indicate low or high byte data transfers. It is used to select latched or immediate data out of the CPU low byte bus transceiver. It also enables low byte parity checking.
XDATADIR	22	I	Transceiver Data Direction - This input is used to select the direction of the peripheral data bus transceiver. When XDATADIR is low, it indicates an I/O read from the XD bus or an interrupt acknowledge cycle. When XDATADIR is high, it indicates data on the SD bus should be placed on XD bus.
AEN	23	I	Address Enable - An active high input that is used to disable the peripheral data bus transceiver while the DMA controller is using the peripheral data bus for address information.
DIR245	11	I	Direction 245 - An input control signal used to set the direction of the high/low system data bus transceiver. This is used for high to low, or low to high data byte moves.
GATE245	12	I	Gate 245 - An active low input that enables the high/low system data transceiver.
–DENHI	21	I	Data Enable High - An active low input that enables a high byte data transfer on the CPU data bus high byte transceiver. When –DENHI is inactive, high byte parity is disabled.
–XBHE	17	I	Transfer Bus High Enable - An active low that indicates a transfer of data on the upper byte of the memory data bus. It also enables high byte parity checking.
–XMEMR	19	I	Memory Read Enable - An active low input signal that indicates when a memory read cycle is occurring. It is used to disable the MDPOUTx signals during a memory write and to latch in the detected parity error signal during a memory read.
MDPOUT0	55	I	Memory Data Parity Out 0 - An active high input that is the output of the stored memory parity data. It is checked for parity errors with the low byte of data read from memory.
MDPOUT1	67	I	Memory Data Parity Out 1 - An active high input that is the output of the stored memory parity data. It is checked for parity errors with the high byte of data read from memory.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
MDPIN0	65	O	Memory Data Parity In 0 - An active high output that is the parity input to the system board memory. It is generated from the current low byte data on the memory data bus.
MDPIN1	8	O	Memory Data Parity In 1 - An active high output that is the parity input to the system board memory. It is generated from the current high byte data on the memory data bus.
PAREN	24	I	Parity Enable - This active high input is used to enable the parity data latch. It is used to prevent false parity errors when ROM memory access occurs.
–PARERROR	15	O	Parity Error - An active low output that is used to indicate that a memory parity error has occurred. This signal is latched by –XMEMR and is valid until the next memory access.
XD0-XD7	46-53	I/O	Peripheral Data Bus Bits 0-7 - I/O's used to control the coprocessor, keyboard, ROM memory, and the DMA controllers.
D0-D15	56-59, 61-64 68, 1-7	I/O	CPU Data Bus Bits 0-15 - This is a bidirectional bus controlled by the DT/–R input.
SD0-SD15	34-31, 29-26, 36-39, 41-44	I/O	System Data Bus Bits 0-15 - These are I/O signals.
VDD	18, 35, 60		System Power: 5 V
VSS	9, 25, 30, 40, 45, 54, 66		System Ground

FUNCTIONAL DESCRIPTION

The VL82C204 is part of a five chip set which together perform all of the on-board logic required to construct an IBM PC/AT-compatible system. The PC/AT-Compatible Data Buffer replaces several bus transceivers and a CPU lower byte data latch located within a PC/AT-type system.

The primary function of the Data Buffer is to multiplex the 80286 microprocessor data lines D0-D15 to the system data bus SD0-SD15 and the peripheral data bus XD0-XD7. This is accomplished through four sets of 8-bit wide data multiplexors. The lower data byte of the CPU data bus transceiver has a byte wide register which is clocked by the rising edge of CNTLOFF. The data can be latched to the lower byte of the CPU data bus only. XA0 is used to control data flow to the CPU data bus. When XA0 = 0, real time data is passed to the CPU data bus. When XA0 = 1, latched data is passed to the CPU data bus. The four groups of transceivers can be seen in the block diagram of the device. The data parity encoder/decoder logic is also located within this device. All data present upon the CPU data bus passes through the parity logic. The outputs of the parity encoder/decoders, MDPIN0 and MDPIN1, are enabled via PAREN to prevent decoding a ROM access and are gated with –XMEMR. The –PARERROR signal is fed back to the Memory Controller where it is gated with other logic to produce the NMI signal for the 80286.

The logic controlling the bus transceivers has been optimized for speed and as such there are no provisions to prevent internal bus collisions. In a standard PC/AT-type application using the full 16 or 20 MHz, the VL82CPCAT-16/-20, chip sets this is not a problem as the control signals which enable the transceivers are decoded in such a fashion as to prevent this from happening. In the case where only the VL82C204 is used, care must be taken as to ensure that the control signals will not cause an internal bus collision. From the block diagram it can be seen that every bus transceiver has an A and B I/O port. The DIR input to the transceiver controls the direction of data flow through the transceiver. A high (1) input into the DIR pin causes data to flow from A to B. A low (0) causes data to flow from B to A. All transceiver enables are low true causing the output of the particular transceiver to be active.

The VL82C204 should be used with either the VL82CPCAT-16 or VL82CPCAT-20 chip sets as it implements a changed architecture from the original system. In order to speed up the memory access, the MD bus (memory data) has been moved to the CPU Data Bus. The VL82C204 has been designed to accommodate this change.

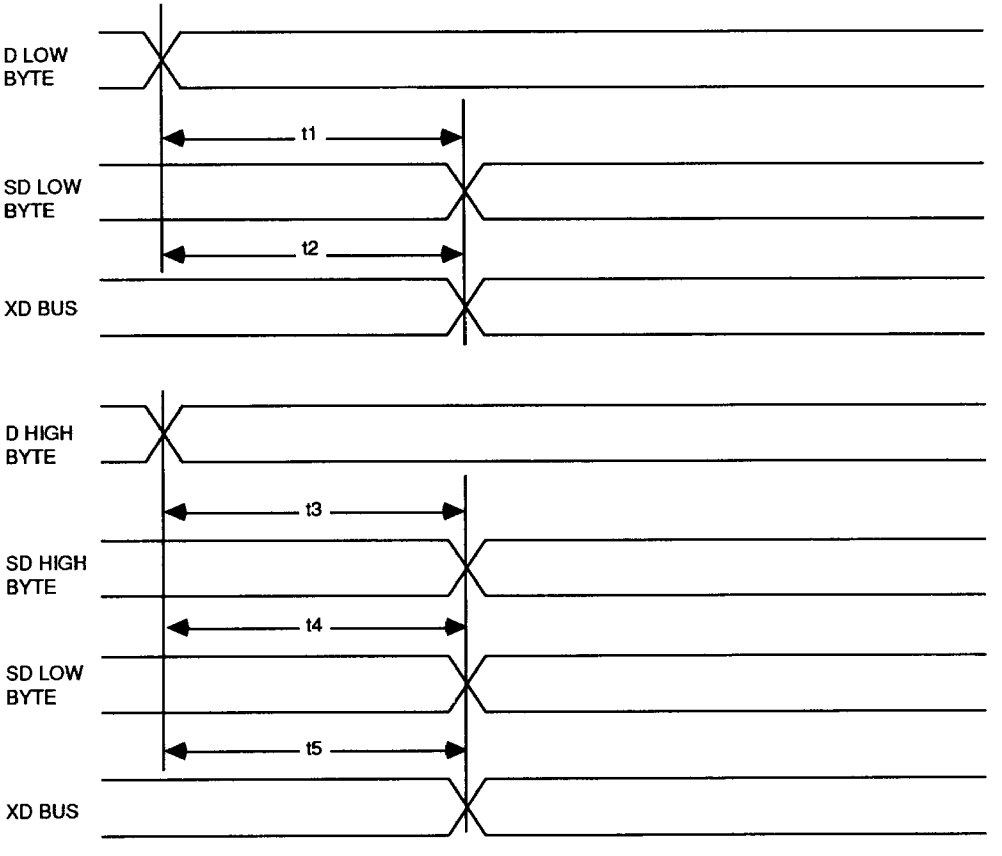
The –TEST pin has been added to enhance system level testing of the chip sets. When this pin is active (0), all outputs and bidirectional pins are placed in three-state. This allows a board level test system to overdrive outputs of the VL82C204 without damage to the device. In addition to three-stating the outputs, all bus control inputs are ignored to prevent internal bus collisions and the internal bus follows the state of the system data bus (SD0-SD15).

AC CHARACTERISTICS: TA = QC: 0°C to +70°C, QI: –40°C to +85°C, VDD = 5 V ±5%, VSS = 0 V

CPU DATA BUS I/O MODE TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
t1	D Low Byte In to SD Low Byte Out		35		35	ns	CL = 200 pF
t2	D Low Byte In to XD Bus Out		30		30	ns	CL = 100 pF
t3	D High Byte In to SD High Byte Out		35		35	ns	CL = 200 pF
t4	D High Byte In to SD Low Byte Out		35		35	ns	CL = 200 pF
t5	D High Byte In to XD Bus Out		30		30	ns	CL = 100 pF

CPU DATA BUS I/O MODE TIMING WAVEFORMS



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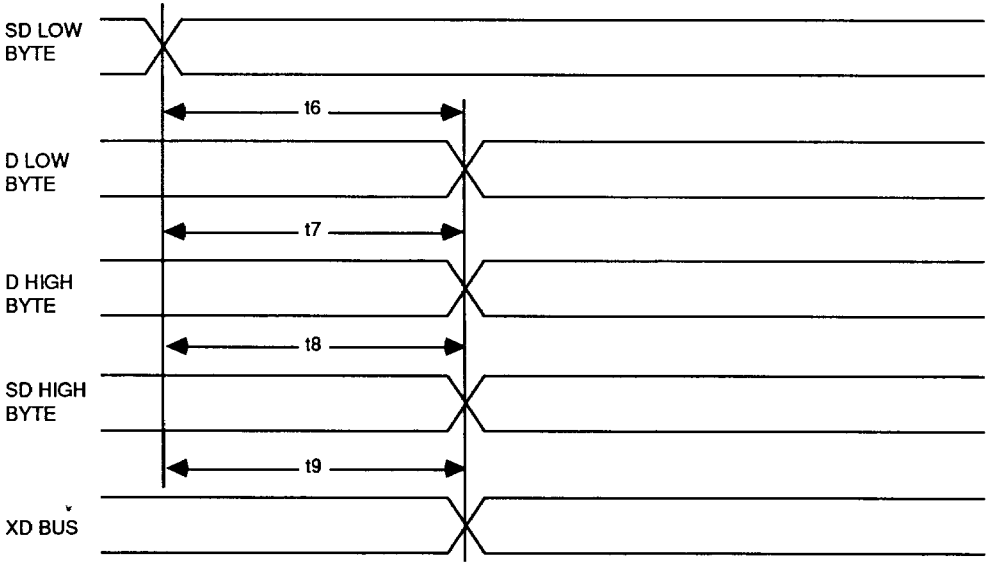
SYSTEM LOW BYTE DATA BUS I/O MODE TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
t6	SD Low Byte In to D Low Byte Out		30		30	ns	CL = 120 pF
t7	SD Low Byte In to D High Byte Out		35		35	ns	CL = 120 pF
t8	SD Low Byte In to SD High Byte Out		35		35	ns	CL = 200 pF
t9	SD Low Byte In to XD Bus Out		30		30	ns	CL = 100 pF

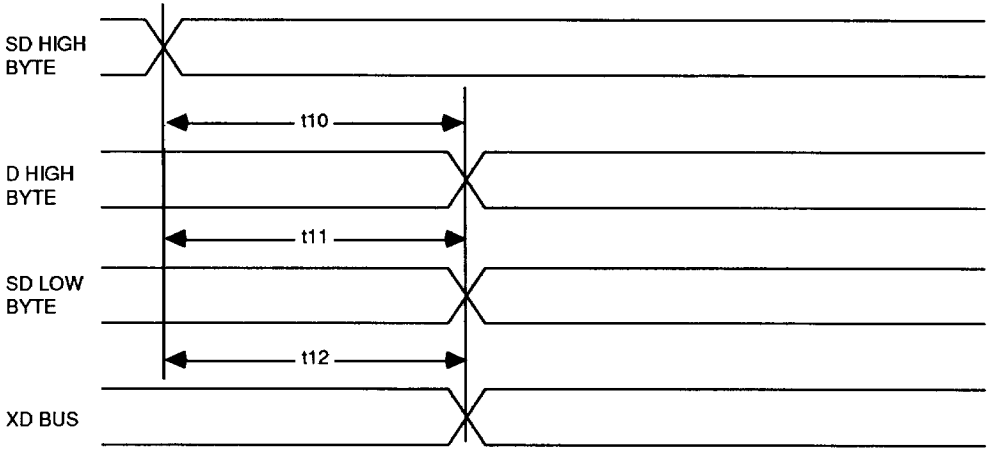
SYSTEM LOW BYTE DATA BUS I/O MODE TIMING WAVEFORMS



SYSTEM HIGH BYTE DATA BUS I/O MODE TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
t10	SD High Byte In to D High Byte Out		30		30	ns	CL = 120 pF
t11	SD High Byte In to SD Low Byte Out		35		35	ns	CL = 200 pF
t12	SD High Byte In to XD Bus Out		30		30	ns	CL = 100 pF

SYSTEM HIGH BYTE DATA BUS I/O MODE TIMING WAVEFORMS



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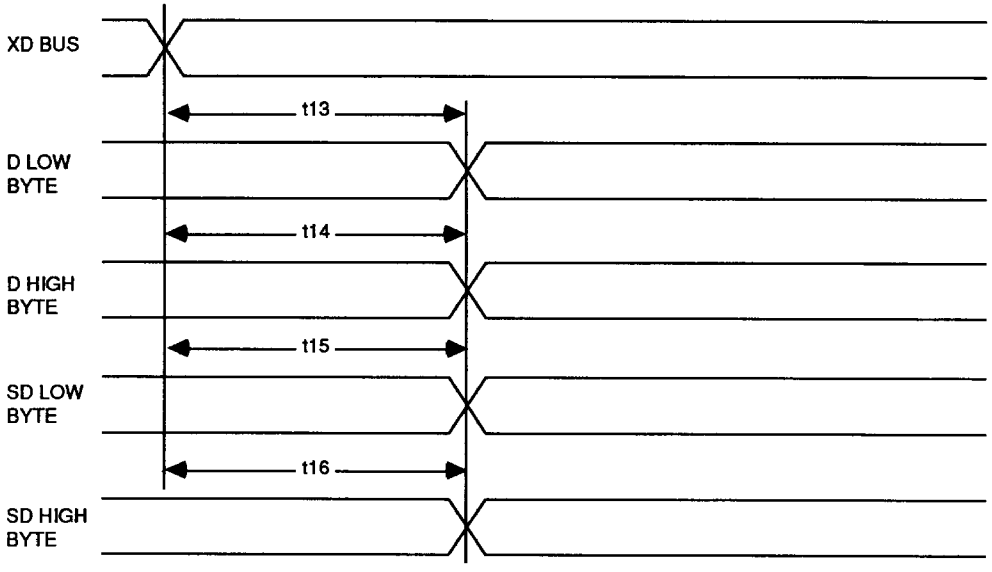
PERIPHERAL DATA BUS I/O MODE TMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
t13	XD Bus In to D Low Byte Out		30		30	ns	CL = 120 pF
t14	XD Bus In to D High Byte Out		30		30	ns	CL = 120 pF
t15	XD Bus In to SD Low Byte Out		35		35	ns	CL = 200 pF
t16	XD Bus In to SD High Byte Out		35		35	ns	CL = 200 pF

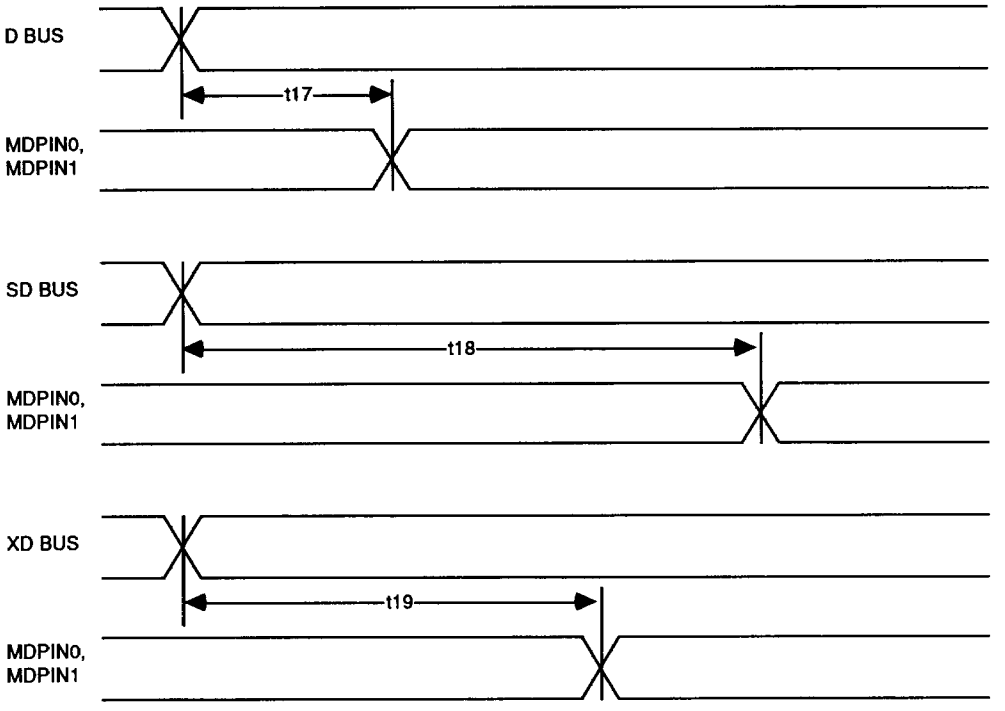
PERIPHERAL DATA BUS I/O MODE TIMING WAVEFORM



MEMORY WRITE MODE TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
t17	D Bus In to MDPIN0, MDPIN1 Out		16		16	ns	CL = 50 pF
t18	SD Bus In to MDPIN0, MDPIN1 Out		46		46	ns	CL = 50 pF
t19	XD Bus In to MDPIN0, MDPIN1 Out		46		46	ns	CL = 50 pF

MEMORY WRITE MODE TIMING WAVEFORM



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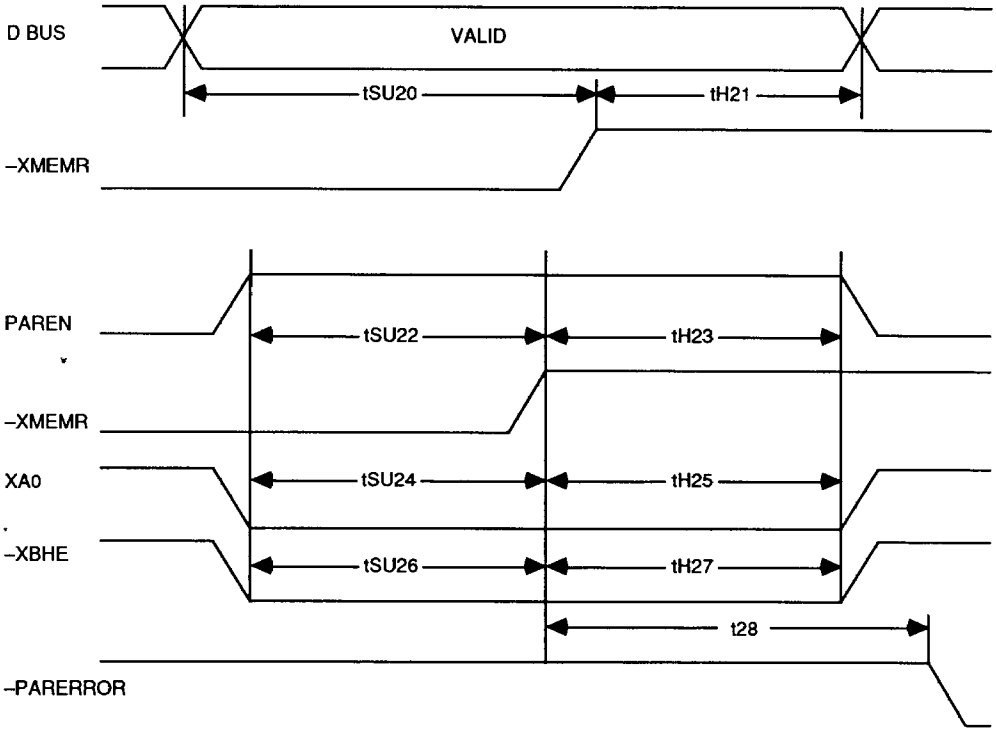
MEMORY READ MODE TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tSU20	D Bus Setup to –XMEMR High	19		19		ns	
tH21	D Bus Hold to –XMEMR High	–4		–4		ns	
tSU22	PAREN Setup to –XMEMR High	10		10		ns	
tH23	PAREN Hold to –XMEMR High	3		3		ns	
tSU24	XA0 Setup to –XMEMR High	10		10		ns	
tH25	XA0 Hold to –XMEMR High	3		3		ns	
tSU26	–XBHE Setup to –XMEMR High	10		10		ns	
tH27	–XBHE Hold to –XMEMR High	3		3		ns	
t28	–XMEMR High to –PARERROR Out		25		25	ns	CL = 50 pF

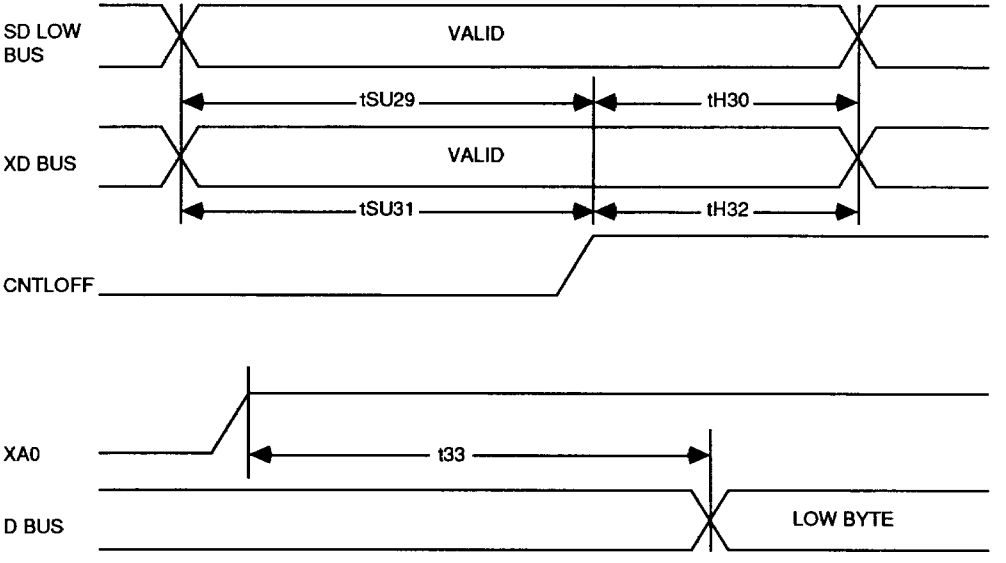
MEMORY READ MODE TIMING WAVEFORM



CPU LOW BYTE DATA BUS LATCH AND SELECT TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tSU29	SD Low Byte Setup to CNTLOFF High	20		20		ns	
tH30	SD Low Byte Hold to CNTLOFF High	10		10		ns	
tSU31	XD Bus Setup to CNTLOFF High	20		20		ns	
tH32	XD Bus Hold to CNTLOFF High	10		10		ns	
t33	XA0 to D Low Bus Out		30		30	ns	CL = 120 pF

CPU LOW BYTE DATA BUS LATCH AND SELECT TIMING WAVEFORMS



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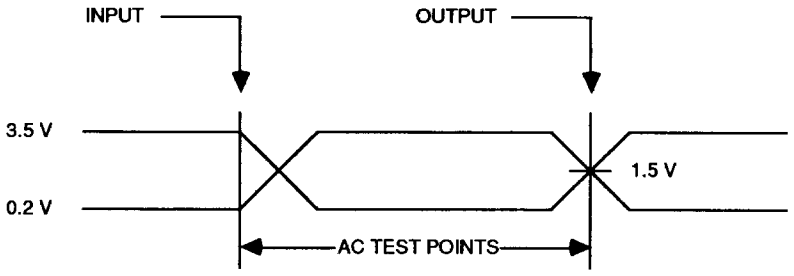
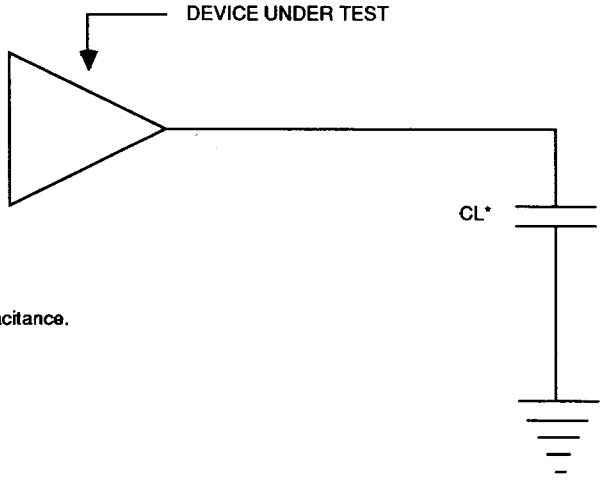
AC TESTING - INPUT, OUTPUT WAVEFORM



AC TESTING - LOAD CIRCUIT



*Includes scope and jig capacitance.

AC TESTING - LOAD VALUES

Test Pin	CL (pF)
26-29, 31-34, 36-39, 41-44	200
1-7, 56-59, 61-64, 68	120
46-53	100
8, 15, 65	50

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	QC = 0°C to +70°C QI = –40°C to +85°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5 V to +7.0 V
Applied Input Voltage	–0.5 V to +7.0 V
Power Dissipation	500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = QC: 0°C to +70°C, QI: –40°C to +85°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
VOH	Output High Voltage	2.4		V	IOH = –3.3 mA
VOL1	Output Low Voltage		0.45	V	IOL = 8 mA, Notes 1 & 3
VOL2	Output Low Voltage		0.45	V	IOL = 24 mA, Notes 2 & 3
VIH	Input High Voltage	2.0	VDD + 0.5	V	
VIL	Input Low Voltage	–0.5	0.8	V	
VIHC	Input High Voltage	3.8	VDD + 0.5	V	CNTLOFF
VILC	Input Low Voltage	–0.5	0.6	V	CNTLOFF
CO	Output Capacitance		8	pF	
CI	Input Capacitance		8	pF	
CIO	Input/Output Capacitance		16	pF	
ILOL	Three-state Leakage Current	–100	100	µA	
ILI	Input Leakage Current	–10	10	µA	
ICC	Power Supply Current		20	mA	@ 1 MHz Test Rate

Notes: 1. Pins 1-7, 46-53, 56-59, 61-64, 68.
2. Pins 26-29, 31-34, 36-39, 41-44.
3. Output low current on all other outputs not mentioned in Note 1 or 2 have IOL (max) = 2 mA.

APPLICATION NOTE

In order to ensure correct function of bus transfers when using the VL82C204 as a stand-alone part (not part of the chip set), the following conditions must be met:

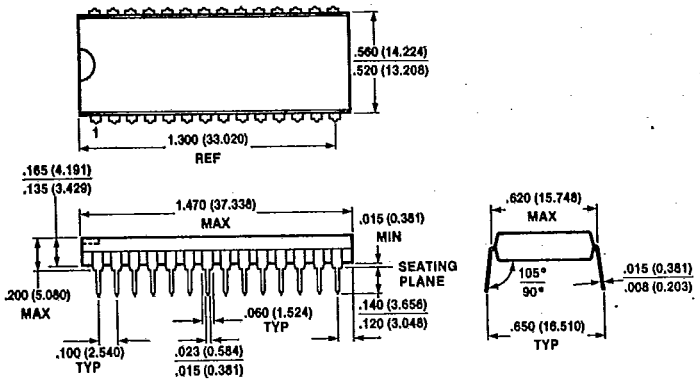
For SD high byte in to SD low byte out, ensure that either –DENHI = 1 or DT/–R = 0.

For SD low byte in to SD high byte out, ensure that either –DENLO = 1 or DT/–R = 0 and AEN = 1 or XDATADIR = 1.

When using the VL82C204 along with the remaining chips in the chip set, these conditions are virtually excluded.

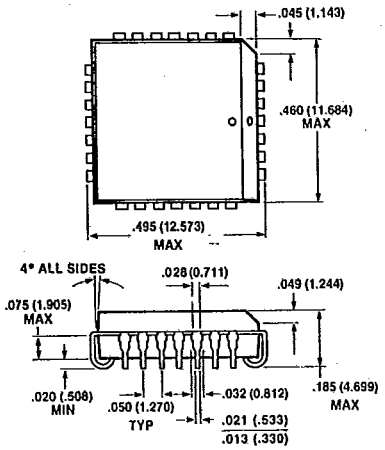
PACKAGE OUTLINES:

28-PIN PLASTIC DUAL IN-LINE



NOTES: UNLESS OTHERWISE SPECIFIED.
1. LEAD FINISH: MATTE TIN PLATE OR LEAD/TIN SOLDER.
2. LEAD MATERIAL: ALLOY 42 OR COPPER.
3. PACKAGE LENGTH DOES NOT INCLUDE END FLASH BURR WHICH IS .010 (0.254) MAX. AT EACH END.
4. TOLERANCE TO BE ± .005 (0.127) UNLESS OTHERWISE NOTED.
5. ALL METRIC DIMENSIONS ARE IN PARENTHESES.
6. PIN 1 INDEX MARK MAY VARY IN SIZE AND SHAPE.

28-PIN PLASTIC LEADED CHIP CARRIER



NOTES: UNLESS OTHERWISE SPECIFIED.
1. TOLERANCE TO BE ± .005 (0.127).
2. LEADFRAME MATERIAL: COPPER.
3. LEAD FINISH: MATTE TIN PLATE OR Sn Pb SOLDER DIP.
4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
6. ALL METRIC DIMENSIONS ARE IN PARENTHESES.

7

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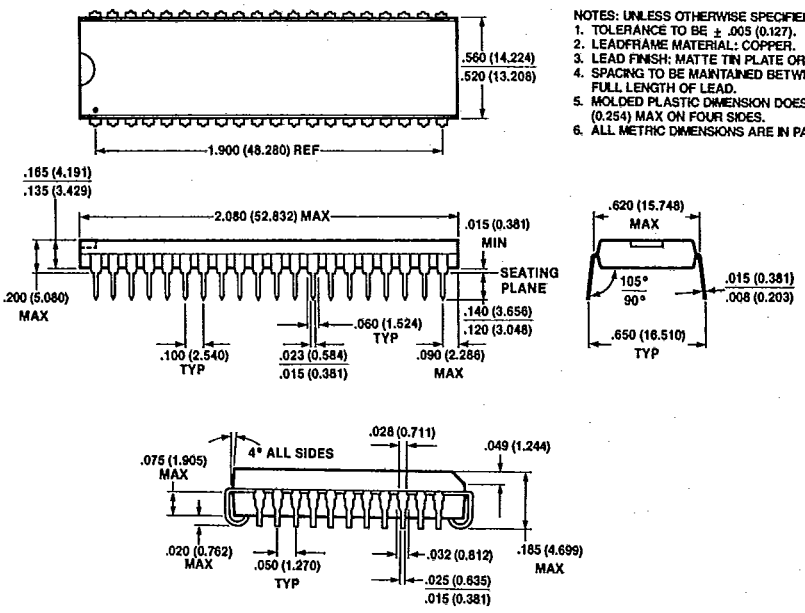
PACKAGE OUTLINES

PACKAGE OUTLINES (Cont.):

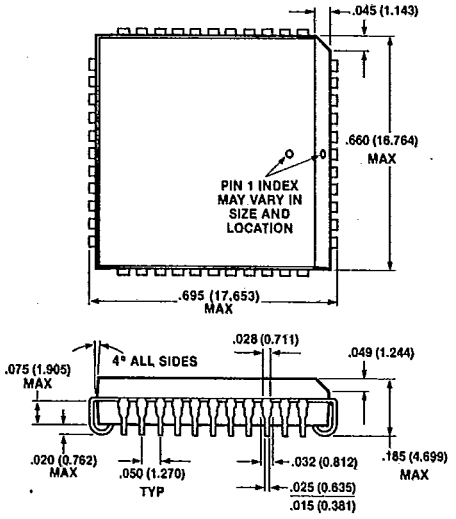
T-90-20

40- PIN PLASTIC DUAL IN-LINE



NOTES: UNLESS OTHERWISE SPECIFIED.
1. TOLERANCE TO BE ± .005 (0.127).
2. LEADFRAME MATERIAL: COPPER.
3. LEAD FINISH: MATTE TIN PLATE OR SOLDER DIP.
4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
6. ALL METRIC DIMENSIONS ARE IN PARENTHESES.

44-PIN PLASTIC LEADED CHIP CARRIER



NOTES: UNLESS OTHERWISE SPECIFIED.
1. TOLERANCE TO BE ± .005 (0.127).
2. LEADFRAME MATERIAL: COPPER.
3. LEAD FINISH: MATTE TIN PLATE OR SOLDER DIP.
4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
6. ALL METRIC DIMENSIONS ARE IN PARENTHESES.

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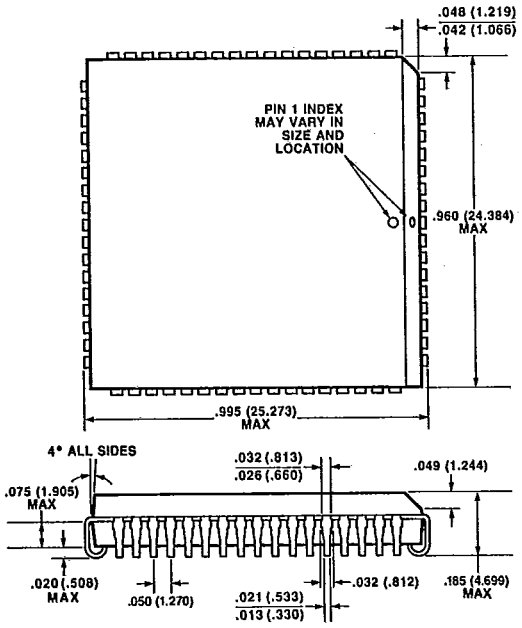
PACKAGE OUTLINES (Cont.):

T-90-20

68-PIN PLASTIC LEADED CHIP CARRIER



7

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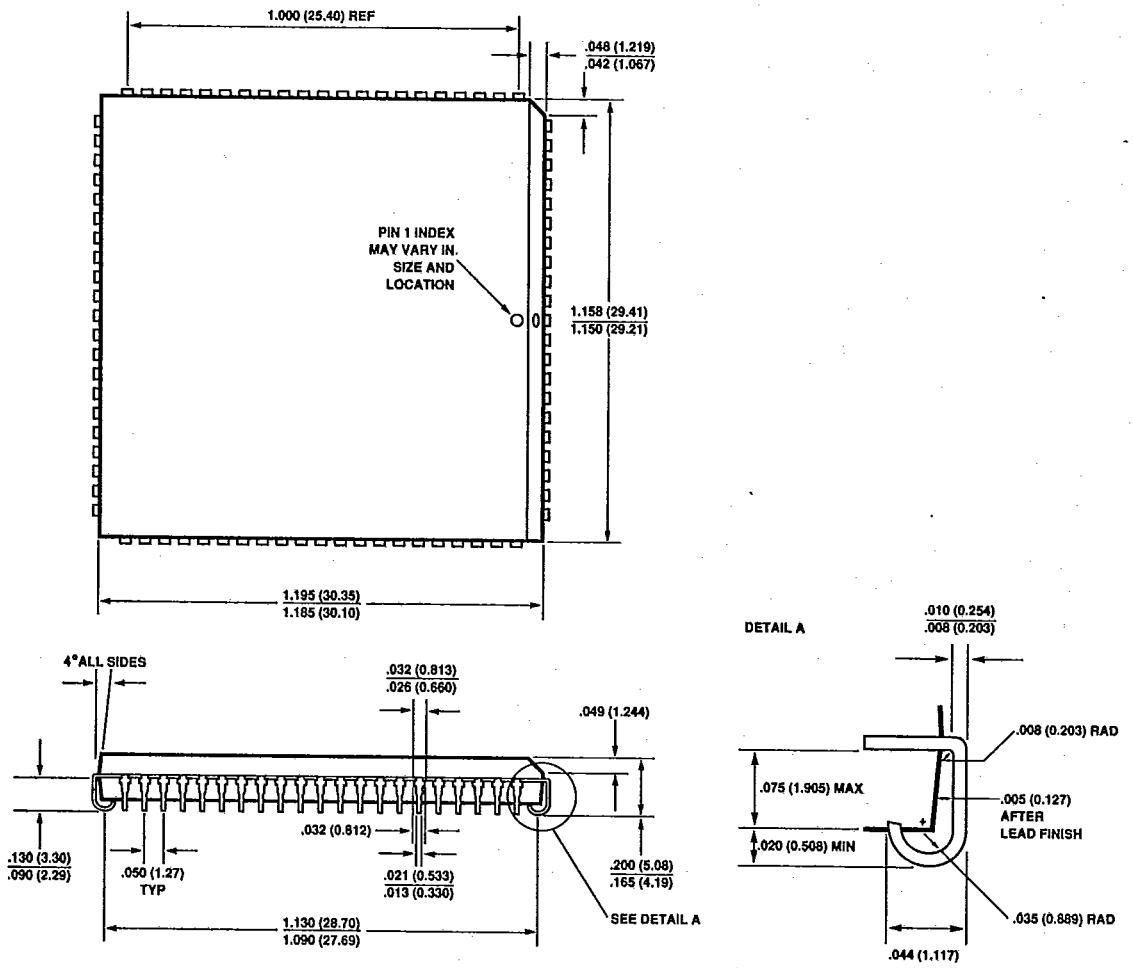
PACKAGE OUTLINES

PACKAGE OUTLINES (Cont.):

T-90-20

84-PIN PLASTIC LEADED CHIP CARRIER



NOTES: UNLESS OTHERWISE SPECIFIED.
1. TOLERANCE TO BE +/- .005 (0.127).
2. LEADFRAME MATERIAL: COPPER.
3. LEAD FINISH: MATTE TIN PLATE OR SOLDER DIP.
4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
6. CONTROLLING DIMENSIONS ARE METRIC, ALL METRIC DIMENSIONS ARE IN PARENTHESES.

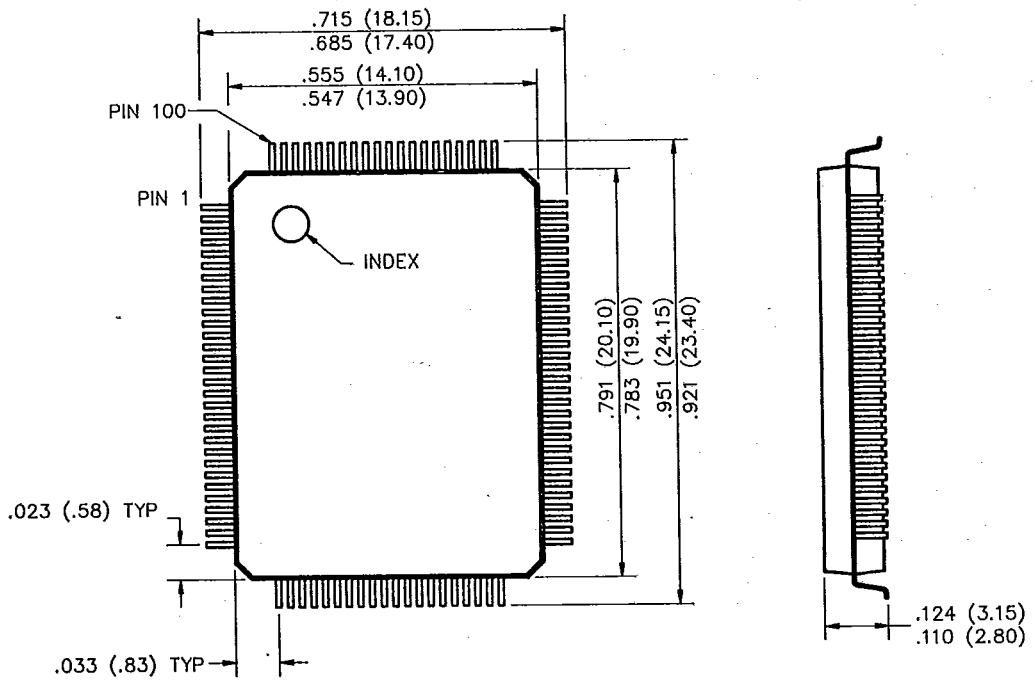
VLSI TECHNOLOGY, INC.

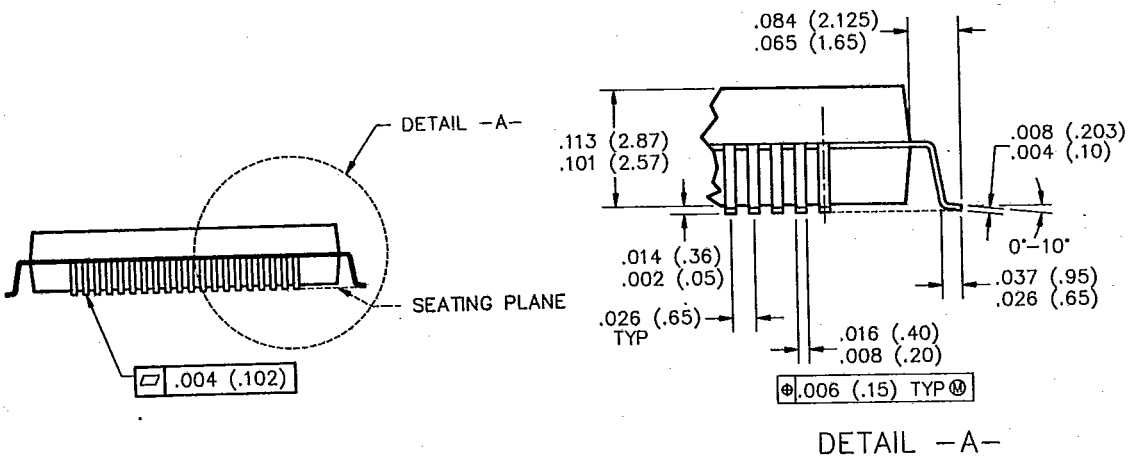
PACKAGE OUTLINES

PACKAGE OUTLINES (Cont.):

T-90-20

100-PIN PLASTIC FLATPACK





DETAIL -A-

NOTES:
1. CONTROLLING DIMENSION IS MM.

7