VL82C102A

PC/AT-COMPATIBLE MEMORY CONTROLLER

FEATURES

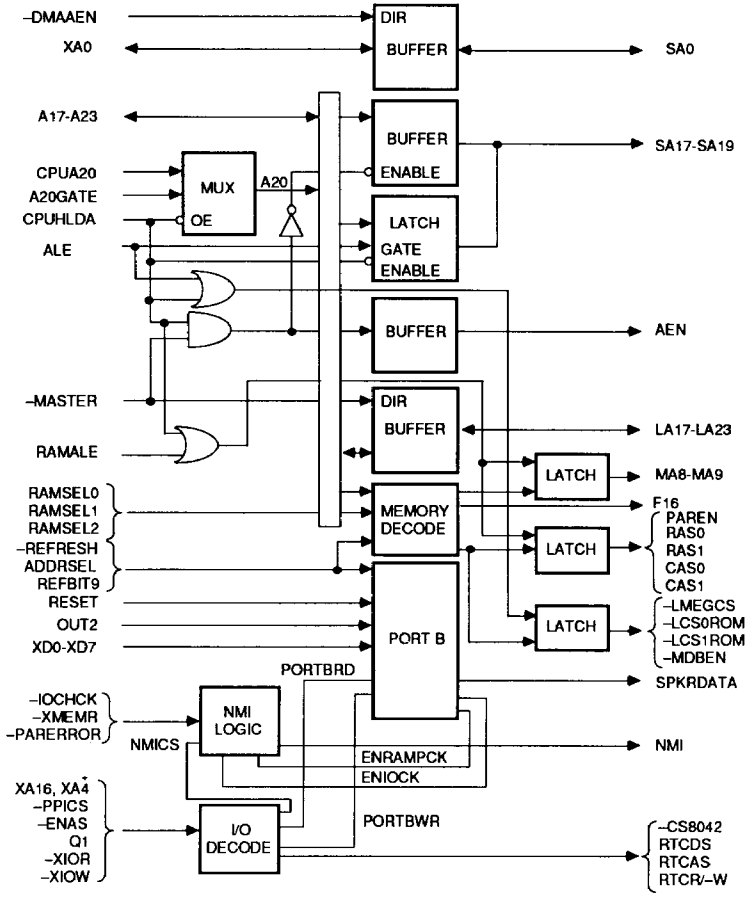
- Fully compatible with IBM PC/AT-type designs
- Completely performs memory control function in IBM PC/AT-compatible systems
- Replaces 20 integrated circuits on PC/AT-type motherboard
- Support 12 MHz system clock
- Device is available as "cores" for user-specific designs
- Designed in CMOS for low power consumption

DESCRIPTION

The VL82C102A PC/AT-Compatible Memory Controller generates the row and column decodes necessary to support the dynamic RAMs used in PC/AT-type systems. In addition, the device allows five motherboard memory options for the user, up to a full 4M-byte system. Four of the five options allow a full 640k-bytes user area to support the disk operating system (DOS). In addition, the VL82C102A provides the upper addresses to the I/O slots, the chip select for the ROM and RAM memory, and drives the system's speaker.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package. The VL82C102A is part of the PC/AT-compatible chip sets available from VLSI. Please refer to the Selector Guide in the front of this manual.

BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL82C102A-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

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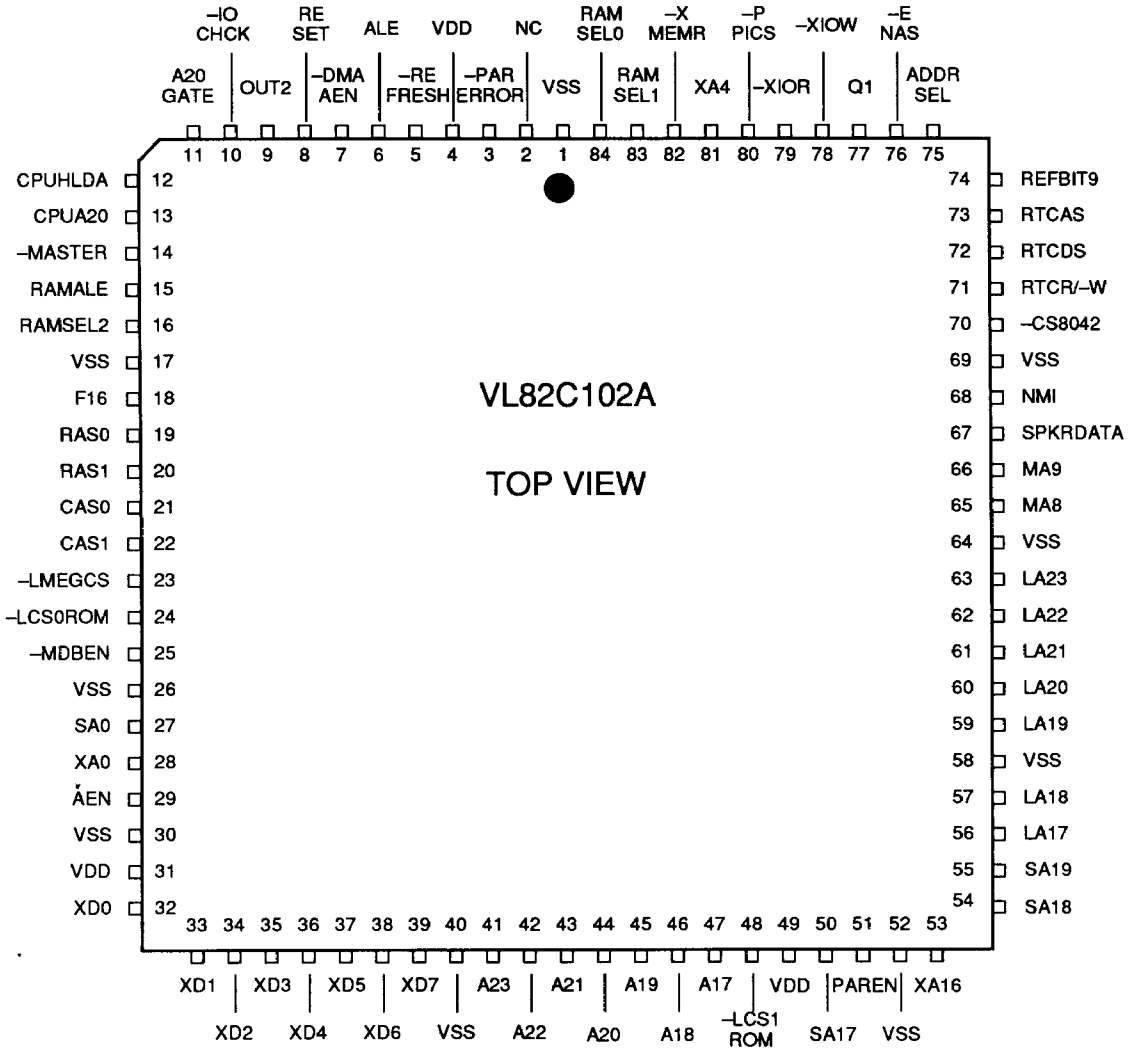
PIN DIAGRAM


VL82C102A
TOP VIEW
11 –IO CHCK
10 A20 GATE
9 OUT2
8 RE SET
7 –DMA AEN
6 ALE
5 –RE FRESH
4 VDD
3 –PAR ERROR
2 NC
1 VSS
84 RAM SEL0
83 RAM SEL1
82 –X MEMR
81 XA4
80 –P PICS
79 –XIOR
78 –XIOW
77 Q1
76 –E NAS
75 ADDR SEL
12 CPUHLDA
13 CPUA20
14 –MASTER
15 RAMALE
16 RAMSEL2
17 VSS
18 F16
19 RAS0
20 RAS1
21 CAS0
22 CAS1
23 –LMEGCS
24 –LCS0ROM
25 –MDBEN
26 VSS
27 SA0
28 XA0
29 AEN
30 VSS
31 VDD
32 XD0
33 XD1
34 XD2
35 XD3
36 XD4
37 XD5
38 XD6
39 XD7
40 VSS
41 A23
42 A22
43 A21
44 A20
45 A19
46 A18
47 A17
48 –LCS1 ROM
49 VDD
50 SA17
51 PAREN
52 VSS
53 XA16
54 SA18
55 SA19
56 LA17
57 LA18
58 VSS
59 LA19
60 LA20
61 LA21
62 LA22
63 LA23
64 VSS
65 MA8
66 MA9
67 SPKRDATA
68 NMI
69 VSS
70 –CS8042
71 RTCR/–W
72 RTCDS
73 RTCAS
74 REFBIT9

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
NC	2		No Connect
–PARERROR	3	I	Parity Error - A low true input used to indicate that a memory parity error has occurred.
–REFRESH	5	I	Refresh - An active low input used to initiate a refresh cycle for the dynamic RAMs.
ALE	6	I	Address Latch Enable - This is a positive edge input that controls the address latches which hold the address during a bus cycle. ALE is not issued for a halt bus cycle.
–DMAAEN	7	I	DMA Address Enable - This is an active low input. It is active whenever an I/O device is making a DMA access to the system memory.
RESET	8	I	Reset - This active high input signal is the system reset generated from a POWERGOOD. It is synchronized to PROCCLK.
OUT2	9	I	Out 2 - The output of the timer controller. It can be read by the CPU on Port B.
–IOCHCK	10	I	I/O Channel Check - This active low input is asserted by devices on the expansion bus. It will generate a non-maskable interrupt if NMI is enabled. –IOCHCK can be read by the CPU on Port B.
A20GATE	11	I	A20GATE - Used to select the proper value for address bit 20. CPUA20 is transmitted out as A20 if A20GATE is high, otherwise A20 is forced low.
CPUHLDA	12	I	CPU Bus Hold Acknowledge - This input indicates ownership of the local CPU bus. When high, this signal indicates that the CPU has three-stated its bus drivers in response to a hold request. When low, it indicates that the CPU bus drivers are active.
CPUA20	13	I	CPU Address Bus Bit 20 - It is transmitted out as A20 if A20GATE is high.
–MASTER	14	I	Master - An active low input. It is asserted low by devices on the expansion bus. A low indicates that another device is active.
RAMALE	15	I	RAM Address Latch Enable - Used in the FASTMODE of operation. When FASTMODE is inactive RAMALE is equal to ALE
RAMSEL2	16	I	RAM Select 2 - Used with RAMSEL0 and RAMSEL1 to select the system RAM configuration.
F16	18	O	An output that indicates a word memory access. It is used to inhibit command delays during a 16 bit memory access.
RAS0	19	O	RAM Address Select 0 - An active high output that is the select signal for the lower address bank of RAM.
RAS1	20	O	RAM Address Select 1 - An active high output that is the select signal for the upper address bank of RAM.
CAS0	21	O	An active high output that is the select signal for the lower bank of RAM.
CAS1	22	O	An active high output that is the select signal for the upper bank of RAM.
–LMEGCS	23	O	Lower Megabyte Chip Select - An active low output that indicates that the lower memory address space (0-1 megabyte) is selected.
–LCS0ROM	24	O	Latched Chip Select 0 for ROM - An active low output that is the latched chip select for the ROM address space.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–MDBEN	25	O	Memory Bus Enable - An active low output that controls the direction of data flow between the system and memory data buses. When –MDBEN is high data flows from memory to system. When low, data flows from system to memory.
SA0	27	I/O	System Address Bus Bit 0 - This signal will be an output with the value of XA0 when –DMAAEN is low. It will be an input and drive XA0 when –DMAAEN = 1.
XA0	28	I/O	Peripheral Address Bus Bit 0 - This signal is an output driven by SA0 when –DMAAEN = 1, and an input driving SA0 when –DMAAEN = 0.
AEN	29	O	Address Enable - This is an output signal for the expansion bus. It will go low when master is active or HLDA is inactive.
XD0-XD3	32-35	I/O	Peripheral Data Bus Bits 0-3 - These are data bits for the peripheral bus. They are outputs when Port B is being read; otherwise they are inputs.
XD4-XD6	36-38	O	Peripheral Data Bus Bits 4-6 - These are data bits for the peripheral bus. They are driven as outputs when Port B is being read, otherwise three-stated.
XD7	39	I/O	Peripheral Data Bus Bit 7 - An output when Port B is read, and an input which enables NMI during an NMICS.
A17-A23	47-41	I/O	CPU Bus Bits 17-23 - These are the upper bits of the CPU address bus. Outputs when –MASTER is low, inputs when –MASTER is high.
–LCS1ROM	48	O	Latched Chip Select 1 for ROM - The active low latched chip select output for the high ROM address space.
PAREN	51	O	Parity check Enabled - Logical OR of CAS0 and CAS1, indicates a memory access so parity check is enabled.
SA17-SA19	50, 54, 55	O	System Address Bus Bits 17-19 - A17-A19 are latched by ALE and transmitted out on these outputs when CPUHLDA is inactive. They are driven directly by A17-A19 when CPUHLDA is active and –MASTER is inactive. They are three-stated when –MASTER is active.
XA16	53	I	Peripheral Address Bus Bit 16 - This switches between –LCS0ROM and –LCS1ROM.
LA17, LA18, LA19-LA23	56, 57 59-63	I/O	System Address Bus Bits 17-23 - These are the upper bits of the system address bus to the expansion slots. These pins are configured as outputs when –MASTER is high, and as inputs when –MASTER is low.
MA8, MA9	65, 66	O	DRAM Memory Address Bus Bits 8-9 - These outputs are the 8th and 9th bit of the DRAM memory address. They are located on the VL82C102A to allow system address mapping. REFBIT9 is multiplexed into MA8 during a refresh cycle.
SPKRDATA	67	O	Speaker Data - Output to be buffered by the 75477 and sent to the speaker.
NMI	71	O	Non-maskable Interrupt - This output is the non-maskable interrupt signal for the CPU.
–CS8042	70	O	Chip Select signal for the Keyboard Controller - This active low output is the chip select signal for the keyboard controller programmable interface device.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–RTCR/W	71	O	Real Time Clock Signal for Read/Write - This is the read/write select output signal for the real time clock. A high indicates a read operation and a low write operation.
RTCDS	72	O	Real Time Clock Data Strobe - This is the data strobe for the real time clock.
RTCAS	73	O	Real Time Clock Address Strobe - This is the address strobe for the real time clock.
REFBIT9	74	I	Refresh Bit 9 - The carry out of the refresh counter. It is used to generate a refresh for 1M DRAMs. It is multiplexed out as MA8 when –REFRESH is active.
ADDRSEL	75	I	Address Select - This input is a multiplex row/column select for the Memory Address Bus drivers.
–ENAS	76	I	Enable Address Strobe - This active low input is used to enable the address strobe on the real time clock. It will go low the first time –S0 is asserted after a system reset.
Q1	77	I	Goes active during the second phase of a CPU bus cycle following the TS state. It is used by the VL82C102A chip to generate the address strobe for the real time clock.
–XIOW	78	I	Input/Output Write - The active low input command to and from the peripheral bus. Used to generate selects for the keyboard controller, real time clock, and Port B.
–XIOR	79	I	Input/Output Read - The active low input command to and from the peripheral bus. Used to generate selects for the keyboard controller, real time clock, and Port B.
–PPICS	80	I	Programmable Peripheral Interface Chip Select - An active low input used to generate the chip select for the keyboard controller.
XA4	81	I	Peripheral Address Bus Bit 4 - An input used to generate selects for the keyboard controller, real time clock, and Port B.
–XMEMR	82	I	Memory Read - An active low input command to and from the peripheral bus. This pin is used to determine the direction of data on the memory data bus and to clock in parity check results.
RAMSEL1	83	I	RAM Select 1 - This input is used with RAMSEL0 to designate the system RAM configuration.
RAMSEL0	84	I	RAM Select 0 - This input is used with RAMSEL1 to designate the system RAM configuration.
VDD	4, 31, 49		System Power: 5 V
VSS	1, 17, 26, 30, 40, 52, 58, 64, 69		System Ground

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FUNCTIONAL DESCRIPTION

The VL82C102A Memory Controller provides address buffering for the upper address bits on the system and CPU address buses. It generates chip selects for the two possible RAM banks and the two possible ROM banks. The VL82C102A also contains the Port B register logic to control the Non-Maskable Interrupt signal and the speaker. It also generates chip select decodes for the keyboard controller and real time clock.

MEMORY DECODES

The upper address bits A17-A23 and XA16 are used to decode chip selects for all on-board memory. The three option inputs RAMSEL2, RAMSEL1, and RAMSEL0 are used to select one of five possible memory mapping options. Refer to Figure 1.

RAM SELECTS

The memory mapping options shown in Figure 1 are used to generate the enable signals for the RAS and CAS pulses to the DRAMs. RAS0 and CAS0 are the enables for Bank 0. RAS1 and CAS1 are the enables for Bank 1. These signals will be active anytime the decode on address bits A17-A23 fall in the ranges shown in the memory maps. The signals are latched by the input signal RAMALE. The latches will be transparent while RAMALE is high and hold the value in the latch while RAMALE is low. The latch clocks will also be forced high when CPUHLDA is active making the latches transparent during all hold acknowledge operations.

When –REFRESH is active, address bits A17-A23 are ignored and both RAS0 and RAS1 are forced active (high) while CAS0 and CAS1 are forced inactive (low).

MA8 AND MA9

A17-A23 are also used to generate four address bits for the upper address bits of the DRAM memory space. These address bits are also latched by the combination of RAMALE and CPUHLDA as described for the RAM selects. The four latched address bits are then multiplexed out on MA8 and MA9. MA9 is needed only if a memory mapping option using 1M-bit DRAMs is selected. REFBIT9 is multiplexed out onto MA8 during refresh cycles.

ROM SELECTS

The ROM address space is decoded from A17-A23 and latched by ALE. These latches are also forced transparent when CPUHLDA is active in the same manner as the latches for the RAM chip selects. This latched value is then split into the two signals –LCS0ROM and –LCS1ROM using the XA16 input. If two banks of 32K by 16-bit words of ROM are used, the XA16 input must by tied to the XA16 signal on the system board to select the proper bank based on the value on XA16. If XA16 is low, –LCS0ROM will go active any time the ROM address space is decoded. If XA16 is high, –LCS1ROM is decoded. In this configuration –LCS0ROM selects the address space from 0E 0000 to 0E FFFF while –LCS1ROM selects the address space 0F 0000 to 0F FFFF. When only using one bank of 16K, 32K, or 64K by 16-bit words of ROM, the XA16 input can be tied high and –LCS1ROM used to select the bank. In this configuration –LCS0ROM will always remain inactive while –LCS1ROM selects the address space 0E 0000 to 0F FFFF.

The ROM address space is duplicated at FE 0000 to FF FFFF and the chip selects will go active in the same manner as described above in this address space.

UPPER ADDRESS BUFFERS

The VL82C102A provides buffer drive capability to drive the card slots on the I/O signals LA17-LA23 and SA17-SA19. The values on A17-A23 are passed directly through to the LA17-LA23 outputs if –MASTER is high. If –MASTER is low LA17-LA23 become inputs and pass the value on those pins to the A17-A23 bus.

A17-A19 are latched by ALE and driven onto the SA17-SA19 bus whenever CPUHLDA is low. When CPUHLDA is high and –MASTER is high, the latch is bypassed and A17-A19 is driven directly to SA17-SA19. SA17-SA19 will be left floating when CPUHLDA is high and –MASTER is low.

ADDRESS BIT 20

Address bit 20 is handled differently than the other address bits. The A20 signal will be generated directly from CPUA20 (which should be connected to A20 on the 80286 CPU) if the input A20GATE is high. If A20GATE is low, the A20 signal is forced low.

ADDRESS BIT 0

A buffer transceiver between XA0 and SA0 is also provided on the VL82C102A. If the input –DMAAEN is high, signal flow is from SA0 to XA0. If –DMAAEN is low, signal flow is from XA0 to SA0.

PORT B

The Port B register in an AT-compatible design is located on the VL82C102A. It can be read or written to with an I/O command to address 61 hex. Port B is used to control the speaker and mask out NMI sources. It can be read to find status of –REFRESH, speaker data, and possible sources of NMI.

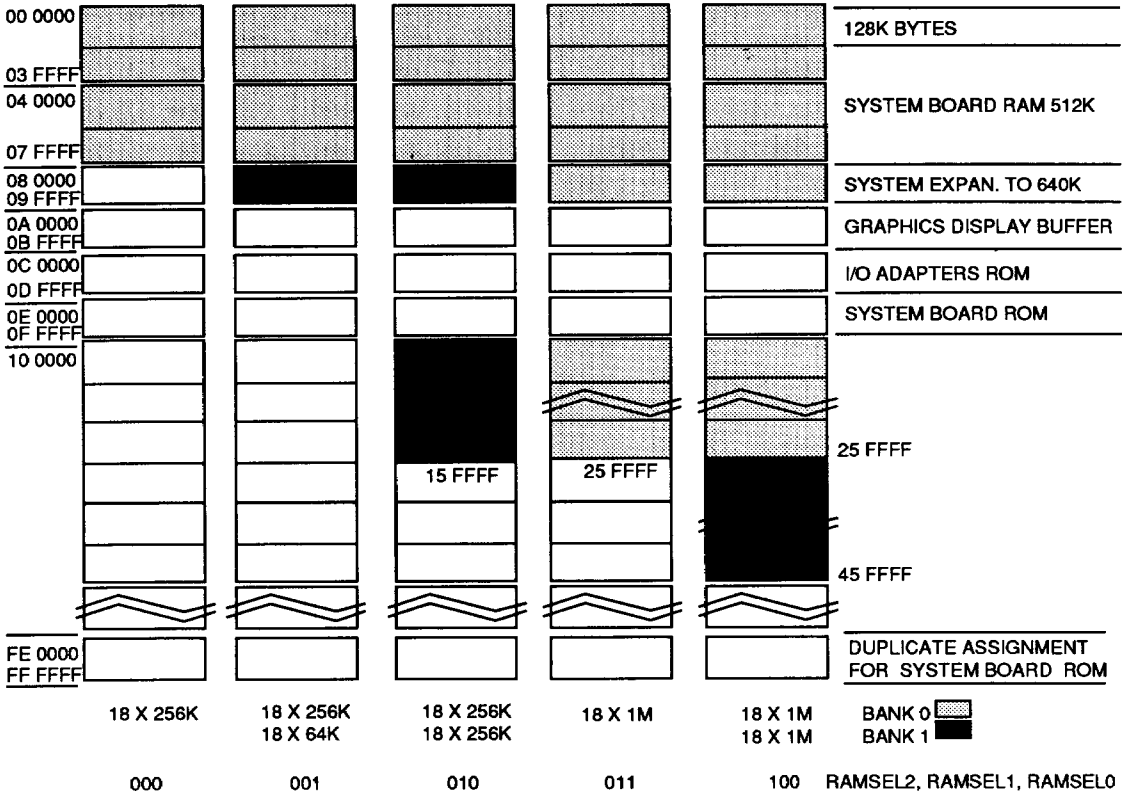
I/O DECODES

The VL82C102A provides the chip select signals for the on-board I/O peripherals (keyboard controller and real time clock).

NMI LOGIC

The logic necessary to control the Non-Maskable Interrupt (NMI) signal to the processor is contained in the VL82C102A. An NMI can be caused by a parity error from the system board DRAM or if an I/O adapter pulls the input IOCHCK low. These two possible sources can be individually enabled to cause an NMI by setting the appropriate bits in the Port B register. At power-up time, the NMI signal is masked off. NMI can be masked on by writing to I/O address 070 hex with bit 7 low, or masked off by writing to I/O address 070 hex with bit 7 high.

FIGURE 1. MEMORY MAP OPTIONS



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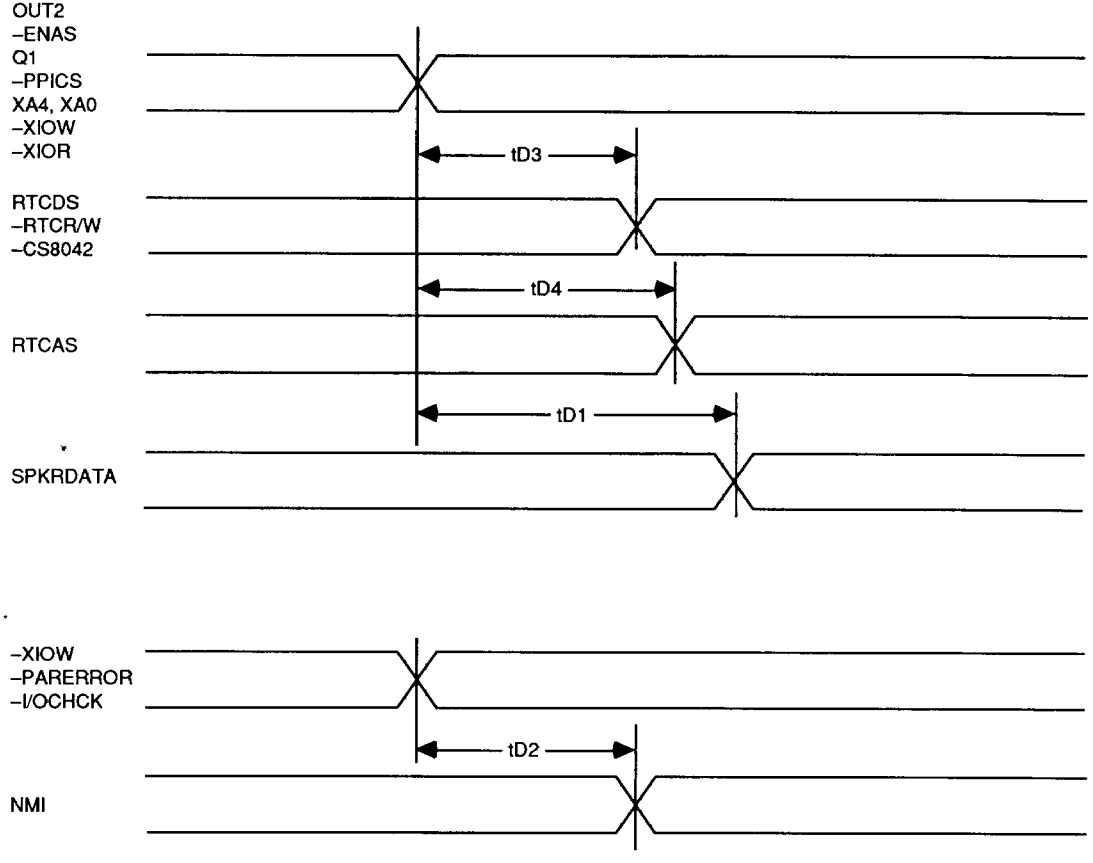
AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ± 5%, VSS = 0 V

PERIPHERAL CONTROL TIMING

Symbol	Parameter	Min	Max	Unit	Condition
tD1	SPKRDATA Output Delay		40	ns	CL = 50 pF
tD2	NMI Output Delay		40	ns	CL = 100 pF
tD3	RTCDS, –RTCR/W, –CS8042 Output Delays		35	ns	CL = 50 pF
tD4	RTCAS Output Delay		40	ns	CL = 50 pF

PERIPHERAL CONTROL TIMING WAVEFORMS

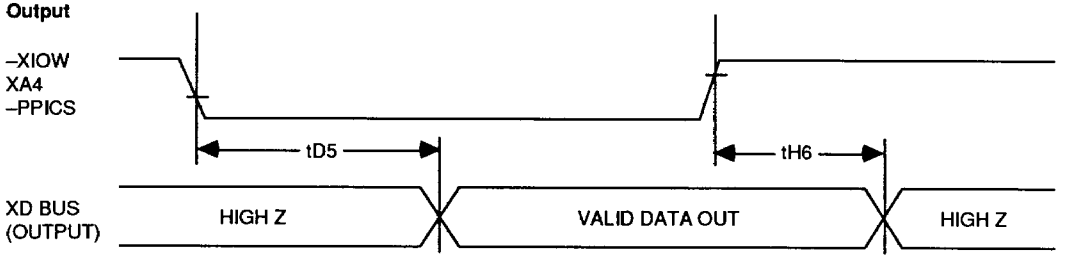


XD BUS TIMING

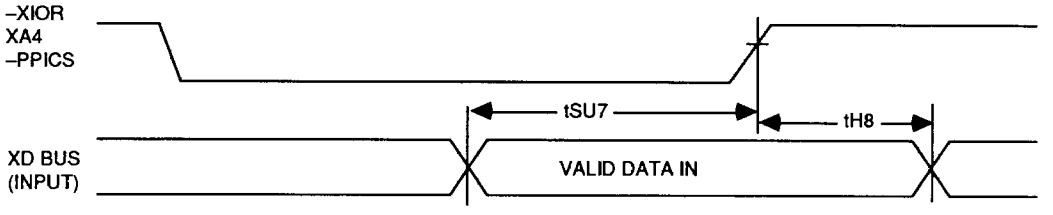
Symbol	Parameter	Min	Max	Unit	Condition
tD5	XD Bus Delay		40	ns	XD = Output
tH6	XD Bus Hold Time	6		ns	XD = Output
tSU7	XD Bus Setup Time	20		ns	XD = Input
tH8	XD Bus Hold Time	12		ns	XD = Input

XD BUS TIMING WAVEFORMS

Output



Input



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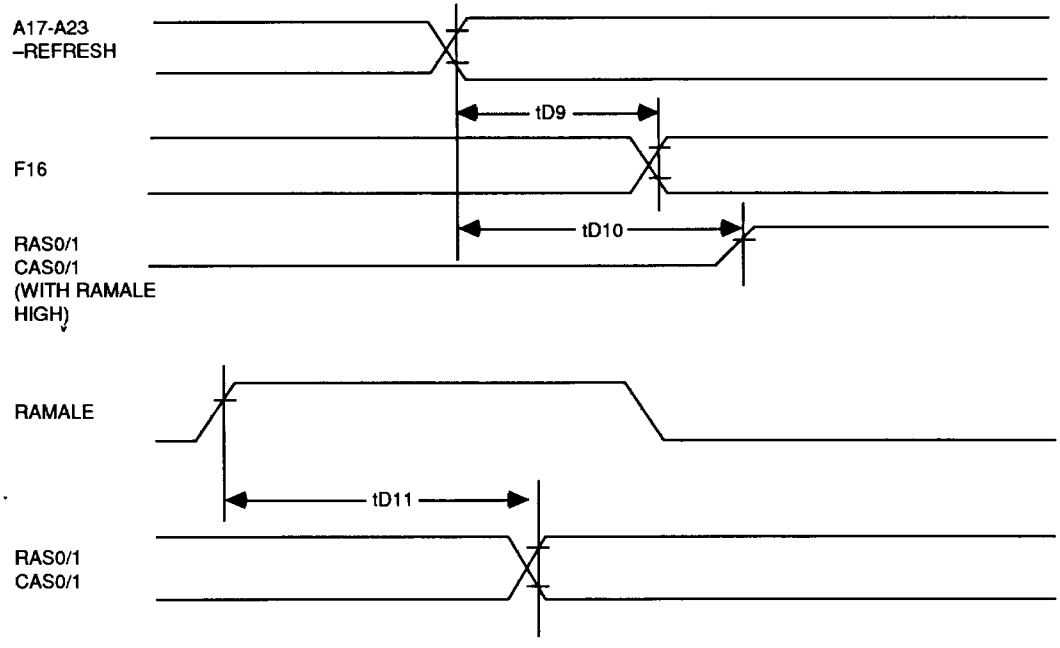
ADDRESS CONTROL TIMING

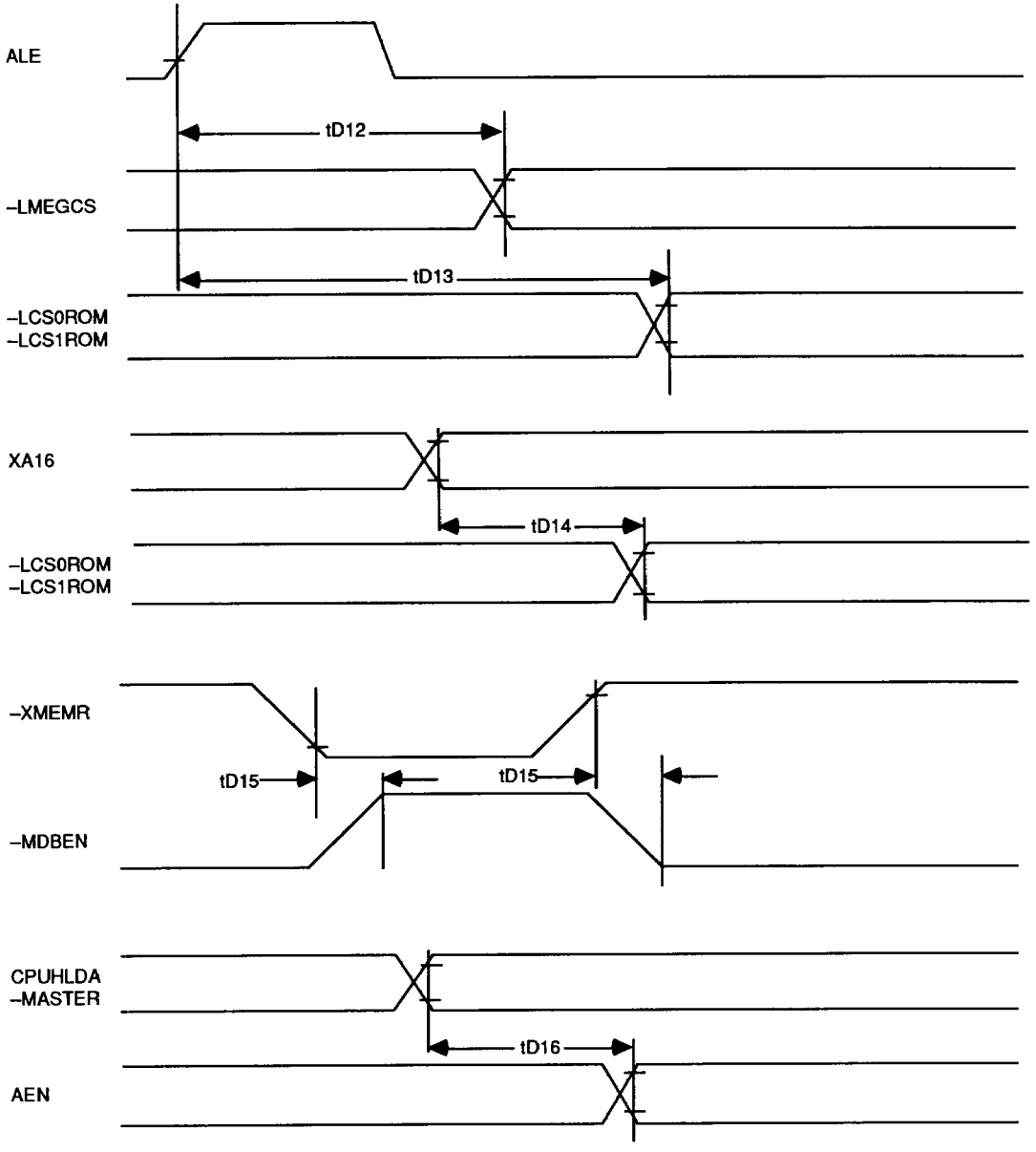
Symbol	Parameter	Min	Max	Unit	Condition
tD9	F16 Output Delay		40	ns	CL = 50 pF
tD10	RAS0/1, CAS0/1 Delay from A17-A23		45	ns	CL = 50 pF, RAMALE High
tD11	RAS0/1, CAS0/1 Delay from RAMALE		24	ns	
tD12	–LMEGCS Delay from ALE		30	ns	CL = 50 pF
tD13	–LCS1ROM, –LCS0ROM Delay from ALE		35	ns	CL = 50 pF
tD14	–LCS1ROM, –LCS0ROM Delay from A16		20	ns	CL = 50 pF
tD15	MDBEN Output Delay		30	ns	CL = 50 pF
tD16	AEN Output Delay		35	ns	CL = 150 pF

Note: RAMSEL0, RAMSEL1, and RAMSEL2 are assumed setup one processor clock before the user generates any memory control signals. These inputs are normally strapped to VDD or VSS in a system.

ADDRESS CONTROL TIMING WAVEFORMS



ADDRESS CONTROL TIMING WAVEFORMS (Cont.)

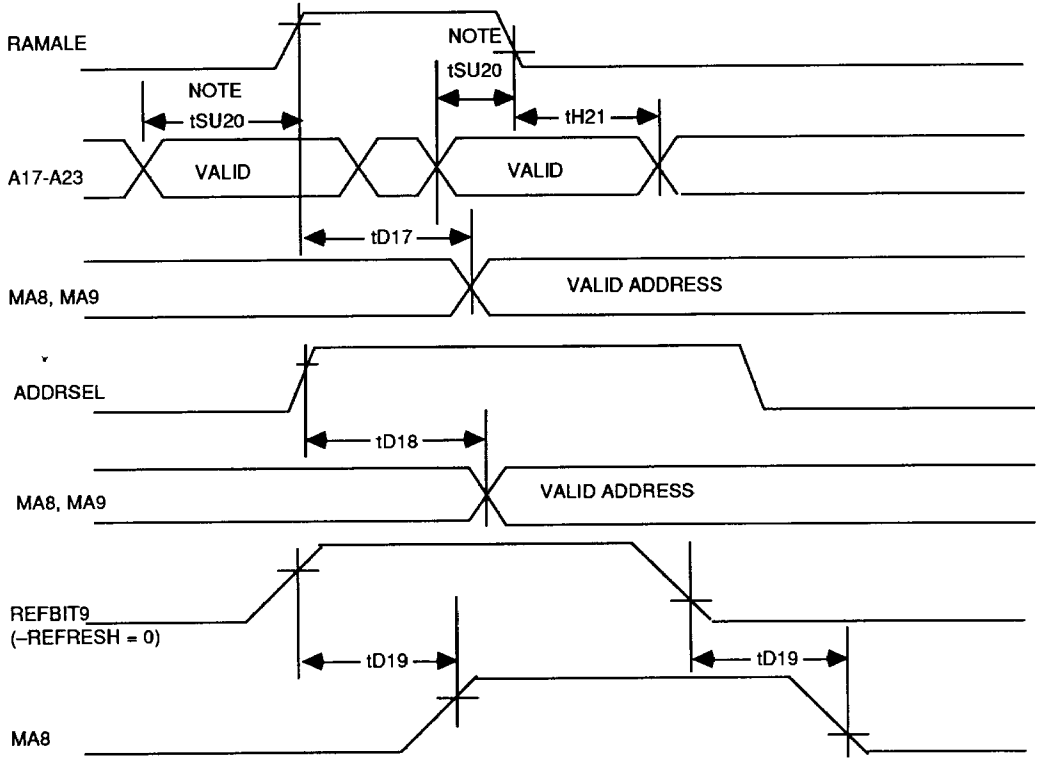


ADDRESS BUS TIMING

Symbol	Parameter	Min	Max	Unit	Condition
tD17	MA8, MA9 Delay from RAMALE		24	ns	CL = 150 pF
tD18	MA8, MA9, Delay from ADDRSEL	6	17	ns	Note, CL = 150 pF
tD19	MA8 Delay from REFBIT9		27	ns	–REFRESH = 0
tSU20	A17-A23 Setup to ALE, RAMALE	45		ns	
tH21	A17-A23 Hold	10		ns	
tD22	XA0/SA0 Delay		35	ns	CL = 50 pF SA0, CL - 100 pF XA0
tD23	SA17-SA19 Delay		40	ns	CL = 200 pF, CPUHLDA = 1, –MASTER = 1
tD24	SA17-SA19 Delay from ALE		35	ns	CL = 200 pF, CPUHLDA = 0
tD25	LA17-LA23 Delay		40		CL = 200 pF, –MASTER = 1
tD26	A17-A23 Delay		40		CL = 50 pF, –MASTER = 0

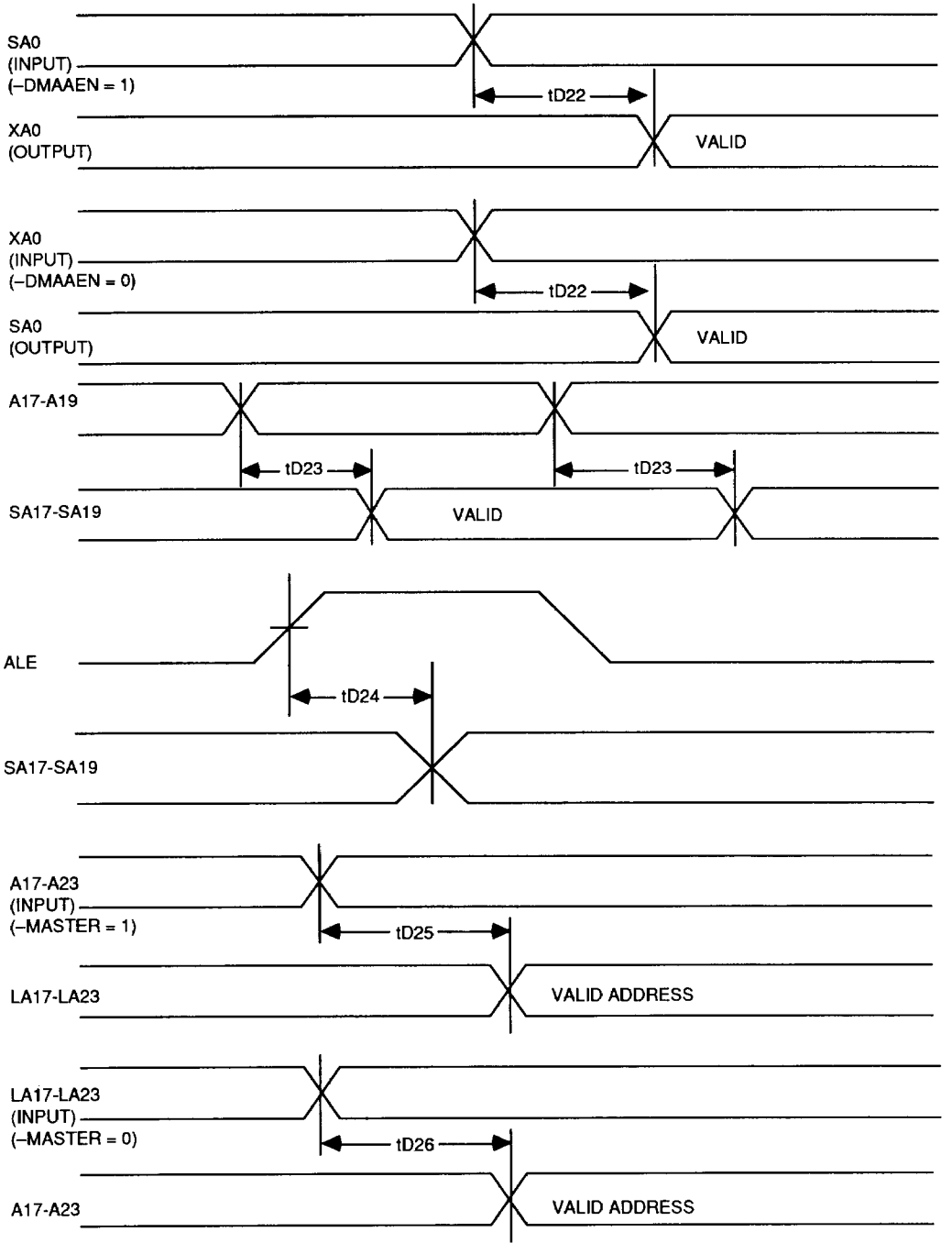
Note: tD18 delay may be derated by a factor of .04 ns/pF for heavier loads.

ADDRESS BUS TIMING WAVEFORMS



Note: tSU20 is specified with respect to the falling edge of RAMALE to guarantee the correct address decodes will be latched in. tSU20 is shown with respect to the rising edge of RAMALE to show time required for address decodes such that propagation delays tD17 and tD11 will be valid. The time does not have to be met with respect to the rising edge for correct functionality.

ADDRESS BUS TIMING WAVEFORMS (Cont.)



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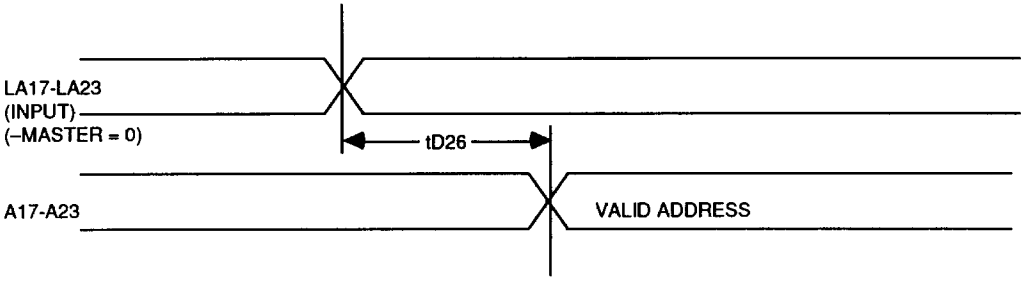
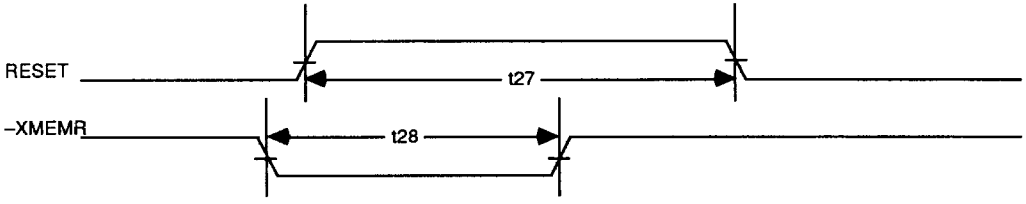
ADDRESS BUS TIMING WAVEFORMS (Cont.)



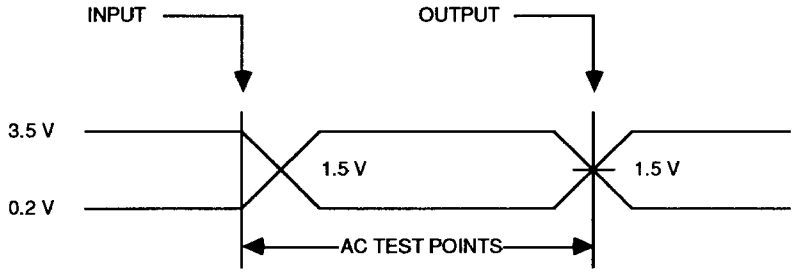
MISCELLANEOUS INPUT TIMING

Symbol	Parameter	Min	Max	Unit	Condition
t27	Min High (Active) Time on RESET	100		ns	
t28	Min Low time for –XMEMR	40		ns	

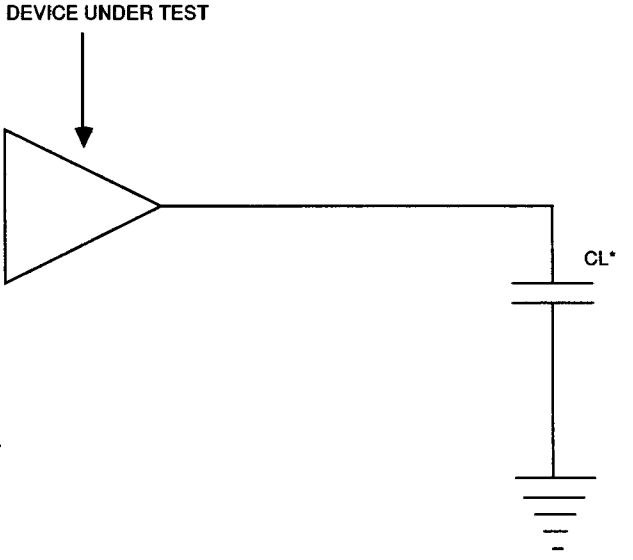
MISCELLANEOUS INPUT TIMING WAVEFORMS



AC TESTING - INPUT, OUTPUT WAVEFORM



AC TESTING - LOAD CIRCUIT



*Includes scope and jig capacitance.

AC TESTING - LOAD VALUES

Test Pin	CL (pF)
27, 29, 50, 54-57, 59-63	200
65, 66	150
28, 32-39	100
All Others	50

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0°C to +70°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5 V to 7.0 V
Applied Input Voltage	–0.5 V to +7.0 V
Power Dissipation	500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

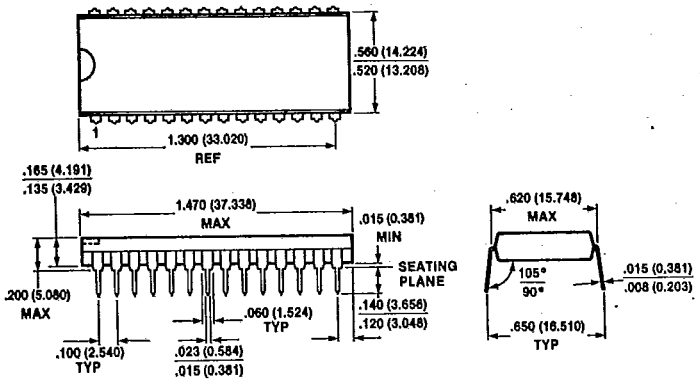
DC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
VOH	Output High Voltage	2.4		V	IOH = –3.3 mA
VOL1	Output Low Voltage		0.45	V	SA0, SA17-SA19, AEN, LA17-LA23, IOL = 20 mA
VOL2	Output Low Voltage		0.45	V	MA8, MA9, F16, XA0, XD0-XD7, IOL = 8 mA
VOL3	Output Low Voltage		0.45	V	All Other Pins, IOL = 2 mA
VIH	Input High Voltage	2.0	VDD + 0.5	V	Except –REFRESH
VIL	Input Low Voltage	–0.5	0.8	V	Except –REFRESH
VIHS	Input High Voltage	3.5	VDD + 0.5	V	–REFRESH, Schmitt-trigger
VILS	Input Low Voltage	–0.5	0.6	V	–REFRESH, Schmitt-trigger
CO	Output Capacitance		16	pF	
CI	Input Capacitance		8	pF	
CIO	Input/Output Capacitance		16	pF	
ILOL	Three-state Leakage Current	–100	100	µA	
ILI	Input Leakage Current	–10	10	µA	
ICC	Power Supply Current		25	mA	Note

Note: Inputs = VSS or VDD, outputs are not loaded.

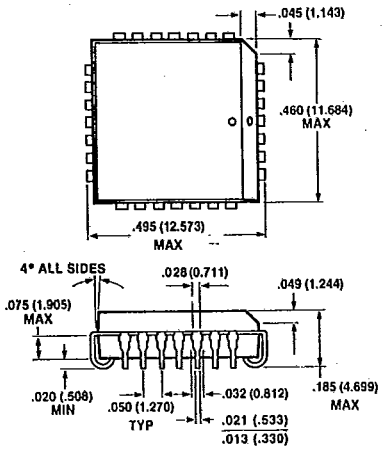
PACKAGE OUTLINES:

28-PIN PLASTIC DUAL IN-LINE



NOTES: UNLESS OTHERWISE SPECIFIED.
1. LEAD FINISH: MATTE TIN PLATE OR LEAD/TIN SOLDER.
2. LEAD MATERIAL: ALLOY 42 OR COPPER.
3. PACKAGE LENGTH DOES NOT INCLUDE END FLASH BURR WHICH IS .010 (0.254) MAX. AT EACH END.
4. TOLERANCE TO BE ± .005 (0.127) UNLESS OTHERWISE NOTED.
5. ALL METRIC DIMENSIONS ARE IN PARENTHESES.
6. PIN 1 INDEX MARK MAY VARY IN SIZE AND SHAPE.

28-PIN PLASTIC LEADED CHIP CARRIER



NOTES: UNLESS OTHERWISE SPECIFIED.
1. TOLERANCE TO BE ± .005 (0.127).
2. LEADFRAME MATERIAL: COPPER.
3. LEAD FINISH: MATTE TIN PLATE OR Sn Pb SOLDER DIP.
4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
6. ALL METRIC DIMENSIONS ARE IN PARENTHESES.

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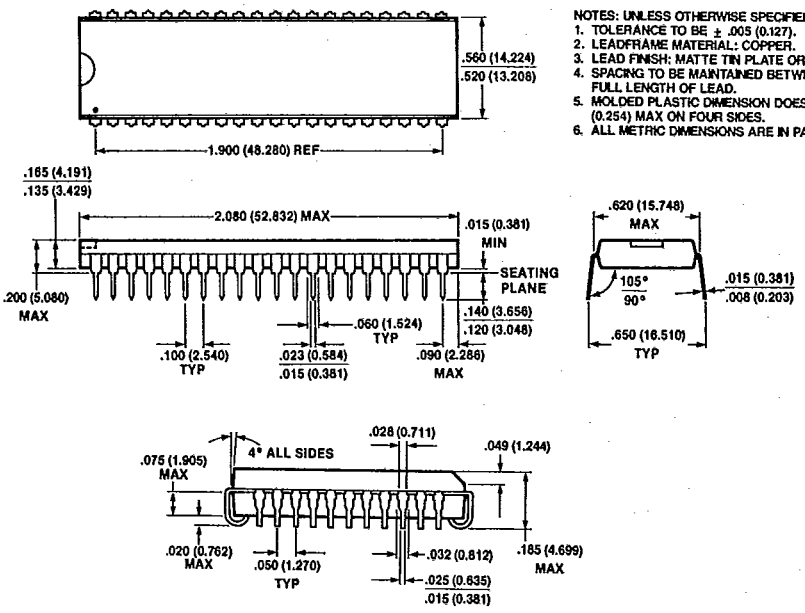
VLSI TECHNOLOGY, INC.

PACKAGE OUTLINES

PACKAGE OUTLINES (Cont.):

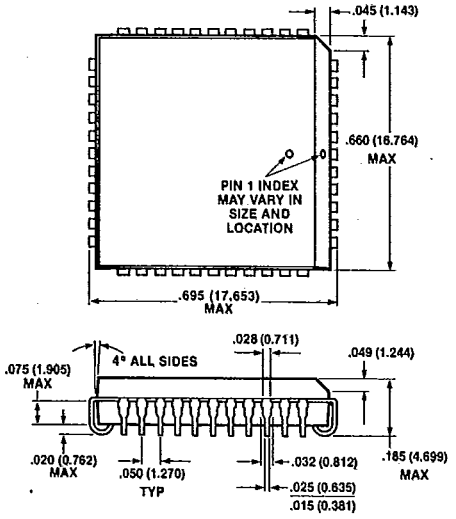
T-90-20

40- PIN PLASTIC DUAL IN-LINE



NOTES: UNLESS OTHERWISE SPECIFIED.
1. TOLERANCE TO BE ± .005 (0.127).
2. LEADFRAME MATERIAL: COPPER.
3. LEAD FINISH: MATTE TIN PLATE OR SOLDER DIP.
4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
6. ALL METRIC DIMENSIONS ARE IN PARENTHESES.

44-PIN PLASTIC LEADED CHIP CARRIER



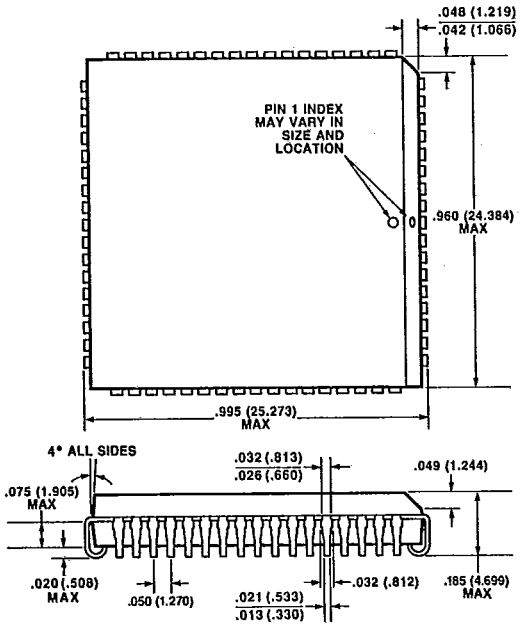
NOTES: UNLESS OTHERWISE SPECIFIED.
1. TOLERANCE TO BE ± .005 (0.127).
2. LEADFRAME MATERIAL: COPPER.
3. LEAD FINISH: MATTE TIN PLATE OR SOLDER DIP.
4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
6. ALL METRIC DIMENSIONS ARE IN PARENTHESES.

VLSI TECHNOLOGY, INC.

PACKAGE OUTLINES (Cont.):

T-90-20

68-PIN PLASTIC LEADED CHIP CARRIER



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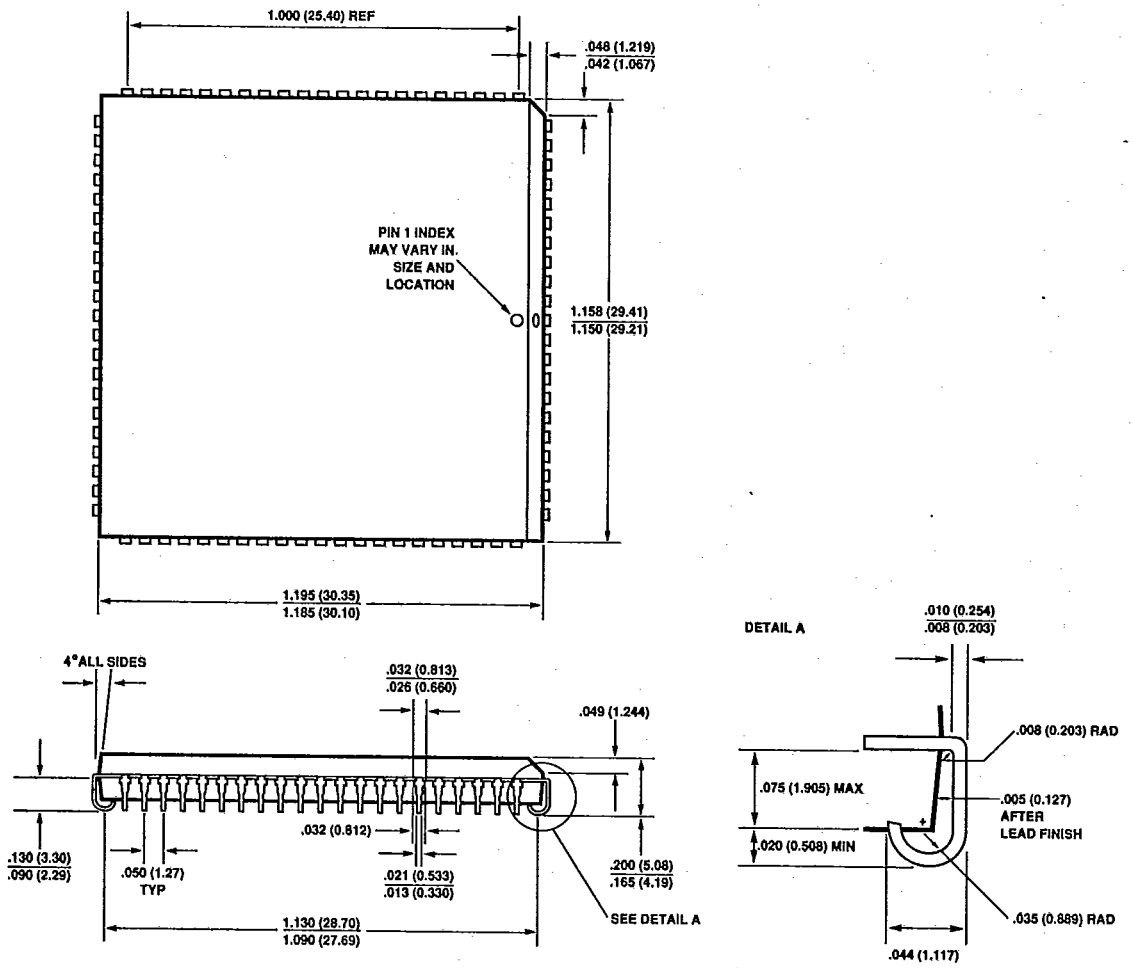
VLSI TECHNOLOGY, INC.

PACKAGE OUTLINES

PACKAGE OUTLINES (Cont.):

T-90-20

84-PIN PLASTIC LEADED CHIP CARRIER



NOTES: UNLESS OTHERWISE SPECIFIED.
1. TOLERANCE TO BE +/- .005 (0.127).
2. LEADFRAME MATERIAL: COPPER.
3. LEAD FINISH: MATTE TIN PLATE OR SOLDER DIP.
4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
6. CONTROLLING DIMENSIONS ARE METRIC, ALL METRIC DIMENSIONS ARE IN PARENTHESES.

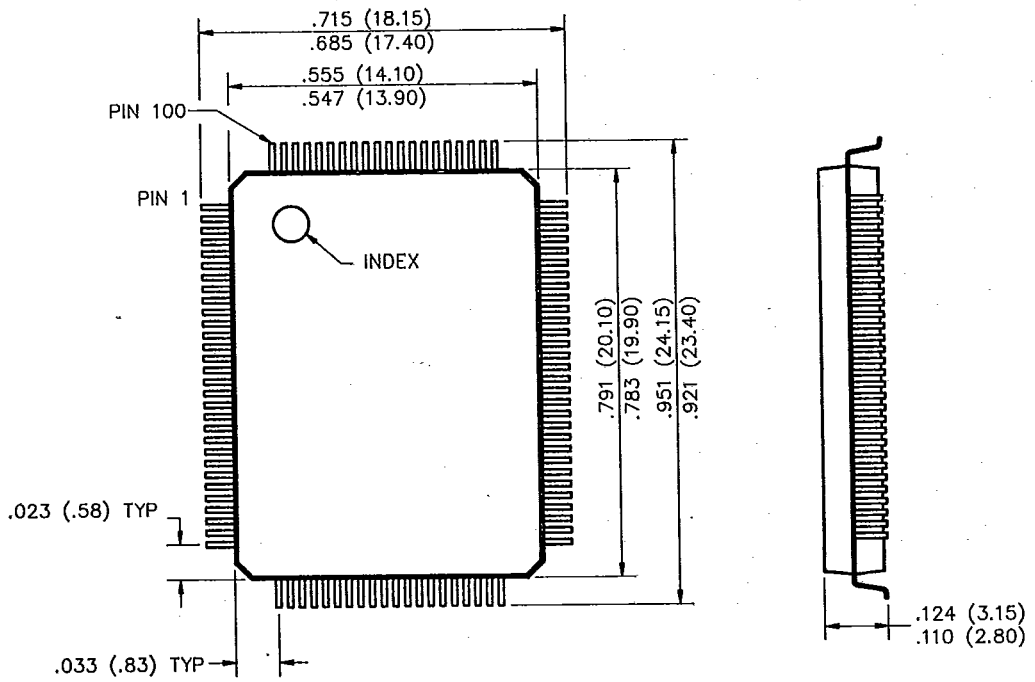
VLSI TECHNOLOGY, INC.

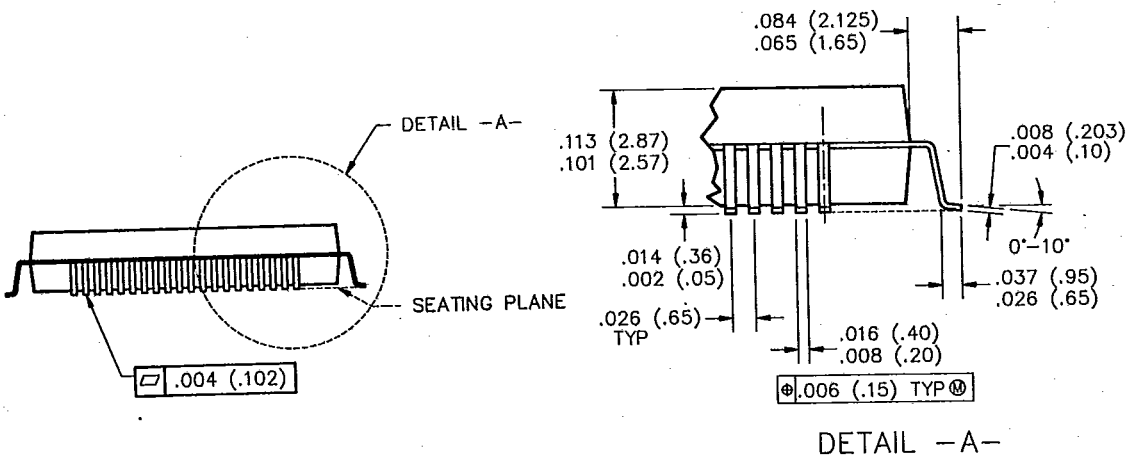
PACKAGE OUTLINES

PACKAGE OUTLINES (Cont.):

T-90-20

100-PIN PLASTIC FLATPACK





DETAIL -A-

NOTES:
1. CONTROLLING DIMENSION IS MM.

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