80286-Based AT Compatible CPU Core Logic

T-49-17-01

FE3500

Features

- 100% IBM® AT® hardware and software compatible
- 6, 8, 10 and 12.5 MHz CPU clock rates
- Five-chip core logic implementation for 80286 CPU
- Packaged in low power CMOS
- EGA BIOS mapping

Description

The FE3500 chip set provides all necessary core logic, memory and I/O control to build a completely integrated IBM® AT® compatible motherboard using the 16-bit Intel® 80286 Central Processing Unit.

It permits a fully functional 80286 AT to be consolidated into a very small form factor and provides the means to embed communications, storage and video control functions directly on the motherboard. It is 100% AT hardware and software compatible.

The FE3500 chip set consists of five devices: FE3000A, FE3010, FE3020, FE3030 and FE3040. They operate at software selectable CPU clock rates of 6, 8, 10 and 12.5 MHz.

The FE3500 chip set has 4 programmable I/O decodes that accommodate additional peripheral adapters via an expansion bus. Running at up to 8 MHz, its Direct Memory Access (DMA) logic requires one wait state.

The high level of cohesion and compatibility between devices, all in low-power CMOS, significantly facilitates design and implementation of AT compatible system boards that are smaller, less noisy and consume less power.

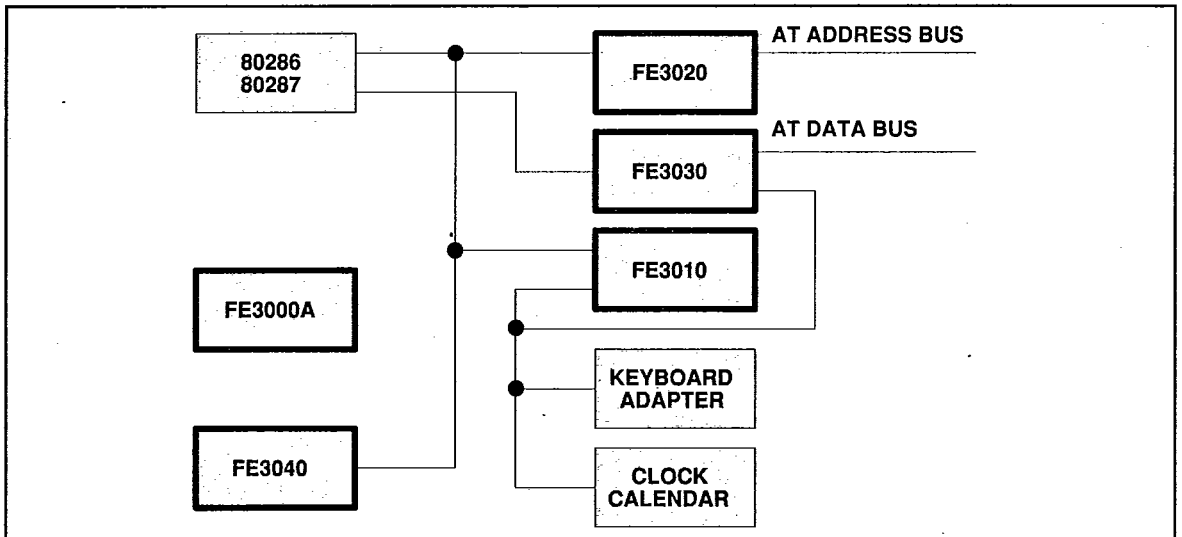
Components

The FE3000A AT CPU Control Logic integrates all control logic supporting the 80286 microprocessor. It contains both processor and coprocessor support logic, wait state generator logic, 256K and 1MB RAM support logic, and operates at 6, 8, 10 and 12.5 MHz clock speeds.

The FE3010 AT Peripheral Control Logic contains 15 interrupt channels, 3 timer channels, 7 DMA channels and supports both 256K and 1MB RAM chips. It supports the 8 MHz DMA operations.

The FE3020 AT Address Buffer Integrated Circuit incorporates address buffers and memory read/write control buffers. The FE3030 Data Buffer Integrated Circuit incorporates the AT system data buffers and control logic.

The FE3040 I/O Manager integrates much of the logic formerly implemented with PALs. It consolidates enhanced multi-speed control logic and decode/mapping logic. It has the ability, through software, to



AT Compatible System

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synchronously change system clock speeds. In addition to reducing component count, the I/O Manager increases functional flexibility and performance by optimizing both system and peripheral clock speeds.

The I/O Manager also provides a Hot Reset feature which permits software conversion from protected mode to real mode without a hard reset.

Clock Speed Management

The FE3040 I/O Manager chip generates chip select decodes for system board resident peripheral chips like the floppy controller, hard disk controller, serial port chip or parallel port chip.

It decouples the peripheral bus to support programmable bus speeds and wait states. This enables full speed CPU local operations with only selected bus accesses running at slower compatibility speeds. Early generation of the IOCS16 signal provides for the critical 16-bit I/O peripheral timing path in high-speed AT compatibles. Overall system performance is greatly enhanced.

Enhanced BIOS Management

Both EGA BIOS and system BIOS can be placed into the same pair of ROM chips or share a single 16-bit wide ROM. The I/O Manager can map the BIOS from slower ROM to faster read-only designated RAM on power-up. It can also split the 8-bit EGA BIOS into 16-bits for faster execution.

Memory Management

The FE3500 chip set supports the DOS defined 640K of memory in 64K block increments on the local bus. Either 256K or 64K RAMs can be used depending on system cost and configuration objectives. The BIOS EPROM resides on the local bus in the top 64K of memory.

A Cost Effective Design

The FE3500 chip set is cost effective because it reduces overall component count, board space and power requirements.

Fully functional AT motherboard circuitry can be consolidated into a very small form factor (less than 35 square inches) leaving sufficient room in most designs to embed additional functions such as standardized floppy, hard disk, video, communications and imaging control. The FE3500 chip set provides exceptional flexibility.

All programmable characteristics may be changed by different versions of BIOS ROMs or through a BIOS ROM set-up program. This programmability greatly reduces the number of required configuration jumpers on the system board. A system configuration register eliminates external dip-switches.

Packaging

The FE3000A, FE3010, FE3020 and FE3030 are packaged in 84-pin, J-leaded surface-mountable plastic chip carriers. The FE3040 is packaged in a 68-pin, J-leaded surface-mountable plastic chip carrier.

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