Biostar MB-8433UUD

Socket 3, 486 Motherboard (UMC 8881/8886)

Manual revision 2.0

Overview

The MB-8433UUD is a generic, 486-class, PCI/ISA motherboard from Biostar Microtech of Taiwan. This company was also known as BMA in the USA, and Bioteq in Europe. Many other companies, including Quantex Computers, MINT-data, Pantex Computer, CyberMax Computers, Pionex Computers, San Carlos Computers, and TC Computers, sold the MB-8433UUD, and other Biostar motherboards, under different names. The MB-8433UUD may have been sold in the USA as MBD-4PB2 and MBD-4MB2. The MB-8433UUD's sold new in 1997 for $99 USD, or about the same price as a PC Chips M919.

The MB-8433UUD was one of the more stable PCI-based 486 motherboards produced. The board is loaded with over-clocking features, boasting a FSB range of 20-83 MHz, and contains the highly sought-after 1:2/3, 1:1/2, and 1:1 FSB-to-PCI multiplier settings. It is one of the few Socket 3, PCI 486-class motherboards to fully support the Intel Pentium Overdrive (POD-83) in write-back (L1) mode. The BIOS firmware designers, and/or UMC chipset designers, also had the foresight to include support for the Cyrix/IBM 5x86 (80-133 MHz) CPU in linear burst mode. This is one of the few motherboards to work reliably with all of Cyrix's 5x86 5th generation features enabled (via software). The motherboard routinely works with an AMD X5-133 @ 160 MHz, and is one of only two boards reported which have successfully run an AMD Am5x86/X5-133 @ 200 MHz (5V). This board works well with all the fastest/overclocked CPU combinations, which include an Am5x86-180 (3x60MHz FSB), Am5x86-133 (2x66MHz), IBM/Cyrix 5x86c-133 (2x66MHz), Intel DX4-120 (2x60 or 3x40 MHz), or an Intel Pentium Overdrive 100 (2.5x40MHz).

In addition to the numerous CPUs supported, the board boasts a working PS/2 mouse port/header and contains an easy-to-modify CPU voltage regulator, allowing for a greater range of CPU core voltages, from 3.0 – 4.0 V with mV tuning. This board also properly supports PCI SCSI bus mastering, which is hard to find on a socket 3 motherboard.

Some of the information contained herein was originally hosted at:
http://www.gweep.net/~sfoskett/hardware/mb8433uud.html and last updated on 6 June 1997. This page was last accessed on 23 June 2004 and saved by Vogons user Feipoa. The e-mail of the author was noted to be sfoskett@slf.gweep.net, however that e-mail address is no longer valid. The information contained in this manual has been heavily modified by Feipoa to the extent that there is little resemblance between the new and old manuals.

Contacts

Biostar had a US office in El Monte, CA but it is apparently no longer open. Biostar distributed in the USA through their subsidiary in Fremont, Asolid Computer Supply. Biostar had webpages at biostar-usa.com in the USA, bioteq.com in Europe, and www.biostar.net and www.biostar.com.tw. Cyrix listed Angelina Shiang (510) 226-6678 as a Biostar contact. Biostar had a BBS at (818) 443-4222 (USA) complete with BIOS updates for all of their motherboards. Quantex Computers had support pages and offered updated BIOSes for this motherboard on their website. Award, the maker of the motherboard's BIOS, mentioned Unicore Software in North Andover, MA, as providing updated BIOS files for Biostar boards.

Award BIOS

This board uses Award's 4.50PG or 4.51PG BIOS. These BIOSes are tweaked by the board manufacturer for the specific motherboard model so Award cannot supply replacements. The latest official BIOS available (960520) uses Award's newer revision, 4.51PG. In 2012, the author modified the BIOS to allow for setting the L2 cache into write-through mode (*L2 Cache Update Scheme*). Other changes included enabling *Load BIOS Defaults*, *Boot Up System Speed*, *PCI/VGA Palette Snoop*, *Delay Before HDD Detection*, *OS Select for DRAM > 64MB*, *ISA Bus Clock Option*, *I/O Recovery Time*, *and Alt Bit in Tag SRAM*. For the Alt Bit, use *7+1* for L2 in write-back mode and *8+0* for L2 in write-through mode. This BIOS message string has also been changed to BIOSTAR MB-8433 v2014.

Whenever you replace/update the BIOS for this board, you should LOAD BIOS DEFAULTS, save, then LOAD SETUP DEFAULTS, save. This is because the options of the new BIOS may differ from your old BIOS and the old settings will still be saved in the real-time clock module. Alternately, you can clear the CMOS data using JP12. BIOS DEFAULTS set the most conservative settings, while SETUP DEFAULTS loads optimal settings. Some users report not being able to get the parallel port working in ECP mode, or more than one serial port working after updating from 960326 to 960520. After resetting the BIOS to default settings, it worked fine. The most common electronically erasable (EEPROM) flash BIOS found on this board was the 5V version from SST, with part number SST PH29EE010-150-3CF. An EEPROM is required to properly flash the BIOS. A Winbond W29EE011-15 or Atmel AT29C010A will also work on the 5 V setting, or an Intel P28F001-BXT150 at 12 V. These flash eraseable BIOSes will also work on most socket 3 motherboards.

The MB-8433UUD BIOS versions are numbered according to their date of issue. For example, UUD960326i represents 26 March 1996. The "i" suffix refers to an Intel (12-volt) EEPROM, while the "s" suffix refers to an SST 5-volt type (*e.g.* part number PH29EE010-150-3CF). The main difference between the two is the memory address where the Plug and Play *ESCD* data is stored. There exist a few SST BIOS chips (PH29EE010-150-3CF) with *SSTGP310* printed on the underside which will not flash for whatever reason. They tend to have a 1996 date code, whereas all BIOS chips with a 1995 date code flashed correctly.

It is important that jumper JP13 be set to the appropriate BIOS ROM type used. If you flash with the wrong BIOS, it may still work but your computer will have Plug and Play problems, particularly with failed detection of PS/2 mouse and serial devices. ESCD also won't save. If you have a BIOS chip with a UV window on the top (EPROM), it cannot be flash programmed in the motherboard; it needs a special UV eraser and programmer. Attempting to flash a UV-erasable BIOS in the motherboard will ruin the BIOS chip.

BIOS Versions

UUD951108A (8 November 1995)

This was apparently the first UUD BIOS found on revision 1 boards. Quantex had these versions on their website.

- UUD951108i - Intel-Style update.
- UUD951108s - SST-Style update.

UUD951205 (5 December 1995)

Pionex Computers had this version on their website. This version was found on revision 1 boards.

- UUD951205s - SST-Style update. Use FLASH.EXE to update the BIOS.

UUD951222 (22 December 1995)

This version seems to have trouble with large (>1024 cylinder) hard disks.

UUD960104 (4 January 1996)

Quantex had this version on their website.

- UUD960104i - Intel-Style update.
- UUD960104s - SST-Style update.

UUD960111 (11 January 1996)

No information available on what features or fixes this version added.

UUD960306 (6 March 1996)

After installing this BIOS version, Windows 95 re-detected the BIOS, hard disk controller, and system board, so it may have fixed/added to these subsystems. Wintune 95 reported no appreciable differences in CPU speed before and after flashing, however the hard disk speed increased by about 20%. Byte's ByteMark benchmark reported nearly identical CPU speeds before and after. This version adds support for an NCR SCSI card, memory parity check function, NEC EDO DRAM.

Quantex had this version on their website.

- UUD960306i - Intel-Style update.

UUD960326 (26 March 1996)

After flashing to this version, Windows 95 redetected the floppy controller, so it may have fixed some sort of floppy bug. [It was noted only to use this BIOS if the U6 chip is marked "74LS244", and not to upgrade if U6 is marked "74F244" – I have found this BIOS to work fine even if U6 is marked 74F244.] The UUD960326 BIOS version is most commonly found on version 3.0 or 3.1 edtions of the motherboard.

This version fixed the following problems:

- Support for AMD 5x86-150 MHz and 160 MHz CPUs. AMD never officially released these CPUs, but if you over-clock your board to run the CPU at 4x 40 MHz, the BIOS reports it as an AMD 5x86-P90 at 160MHz.
- A fix for system boot-up problems when only 1MB of DRAM is installed.

Quantex had these versions on their website:

- UUD960326i - Intel-Style update.
- UUD960326s - SST-Style update.

UUD960520 (20 May 1996)

This BIOS uses an updated version of the AWARD software, version 4.51PG. This version only seems to come in the edition for the SST flash BIOS, UUD960520s. I believe this version fixes a bug with the displaying of "Updating ESCD" at every POST even when the ESCD is not updated. ESCD should only be "updated" when there are hardware, IRQ, or resource changes.

Pantex had this version on their website.

- UUD960520s - SST-Style update.

UUD2012 (16 November 2012)

BIOS version UUD960520 was altered to unhide the following options:

L2 Cache Update Scheme, *Load BIOS Defaults*, *Boot Up System Speed*, *PCI/VGA Palette Snoop*, *Delay Before HDD Detection*, *OS Select for DRAM > 64MB*, *EDO DRAM Read Speed*, *ISA Bus Clock Option*, *I/O Recovery Time*, and *Alt Bit in Tag SRAM*.

UUD2014 (19 September 2012)

BIOS version UUD2012 was altered to rehide *EDO DRAM Read Speed* because this feature was found to non-functional on this motherboard.

UUD586X2 (6 April 2014)

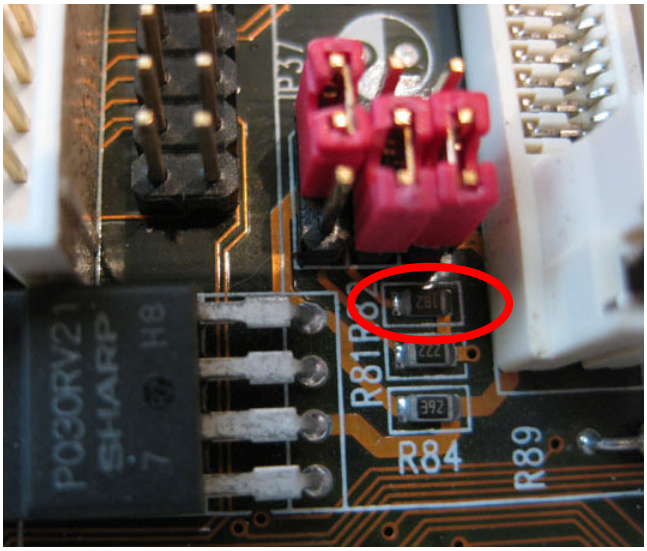
This is the BIOS version UUD2014 but with the default CMOS settings adjusted for stable IBM 5x86c-133 operation with a 66 MHz FSB.

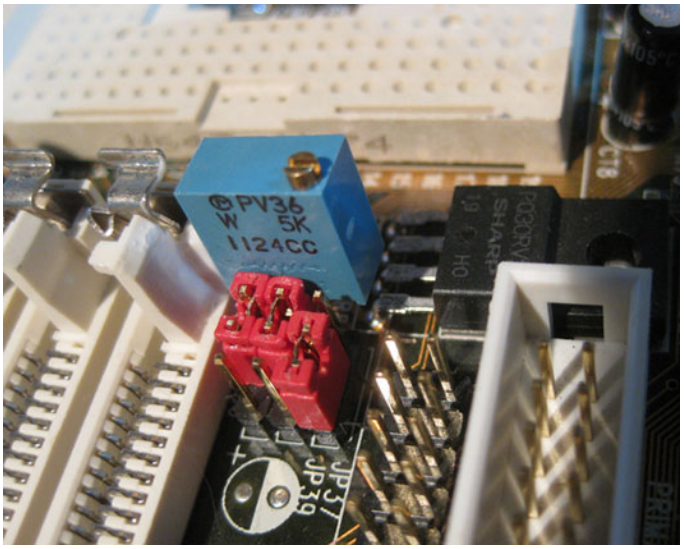
CPU Types

According to the official printed motherboard manual, the MB-8433UUD is capable of 25, 33, and 40 MHz bus speeds, 1×, 2×, 3×, and 4× CPUs, and 25, 26.7, and 33 MHz PCI bus speeds. It supports just about any 486-pinout CPU and is highly configurable. Bench top tests indicate that this board has FSB jumper settings for 20, 25, 33, 40, 50, 60, 66, and 83 MHz. The 60 MHz and 66 MHz settings appear relatively stable using fast cache (10-12 ns) and fast RAM (60 ns). Running the PCI bus at 40 MHz is also sometimes possible, depending on which PCI cards are installed, how much cache you have, and which cache timings you use.

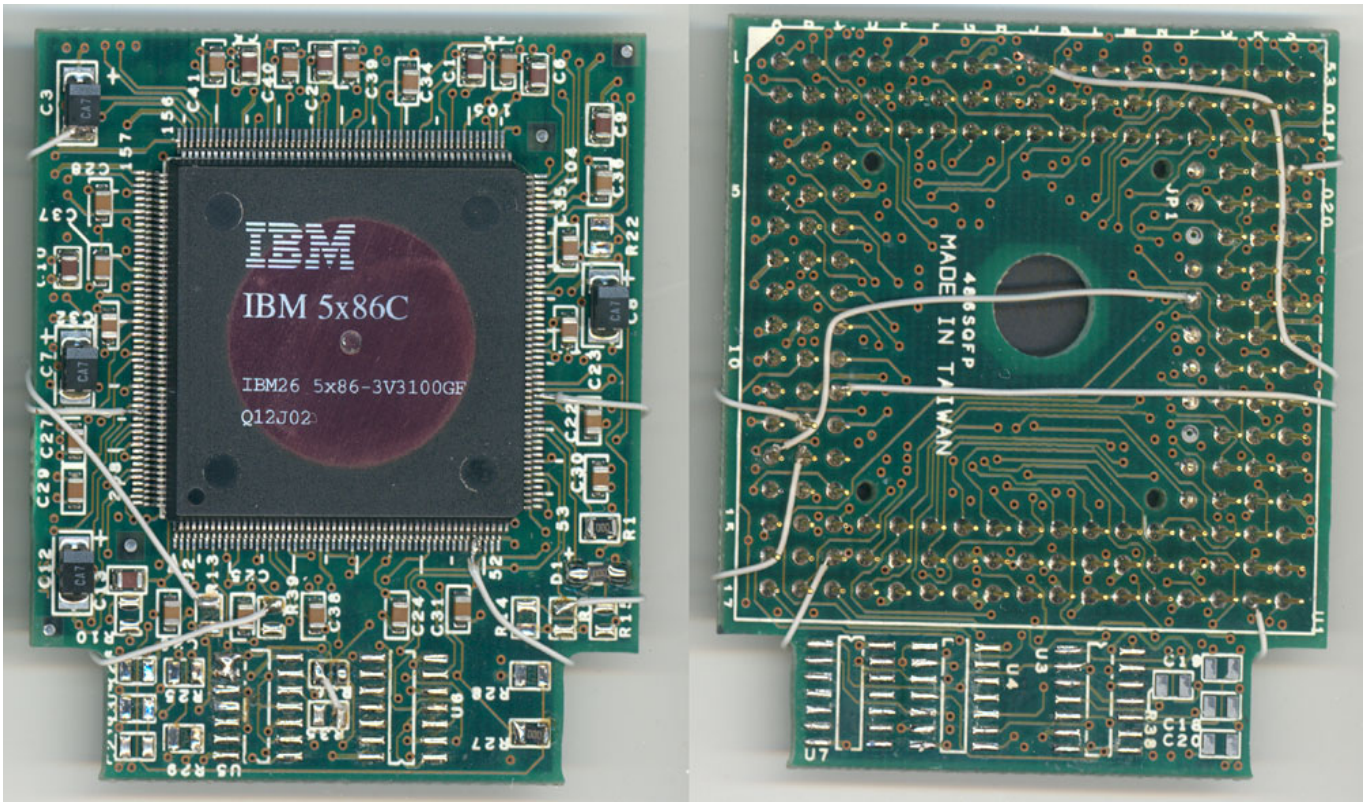
Many IBM 5x86c-100HF CPUs will run reliably at 2 × 66 MHz (133 MHz, 3.75 V) and 2 × 60 MHz (120 MHz, 3.6 V), while some rare AMD X5-133 CPUs will operate as high as 4 × 50 MHz (200 MHz, 5 V). Some Pentium Overdrives, POD83, work

well at 100 MHz using the 40 MHz FSB setting (and in write-back cache mode!). Intel DX4-100 CPUs may also work at 133 MHz using the 2 × 66 MHz and 4 V settings, but tend to overheat quickly. Nearly all Am5x86-133 chips run well at 4x40 MHz and 3x50 MHz while some Am486 DX2-66V16BGC CPUs run at 2x66. The motherboard must be modified to allow for voltages other than 3.45 V, 4.0 V, and 5.0 V. This involves removing the 1.8K SMD resistor responsible for the 4.0 V setting and replacing it with a 5 K-ohm trimmer. This allows for very fine voltage adjustments between 3.0 and 4.1 V. The SMD resistor to be removed is located at R82. More information can be found here, http://www.vogons.org/viewtopic.php?t=30348

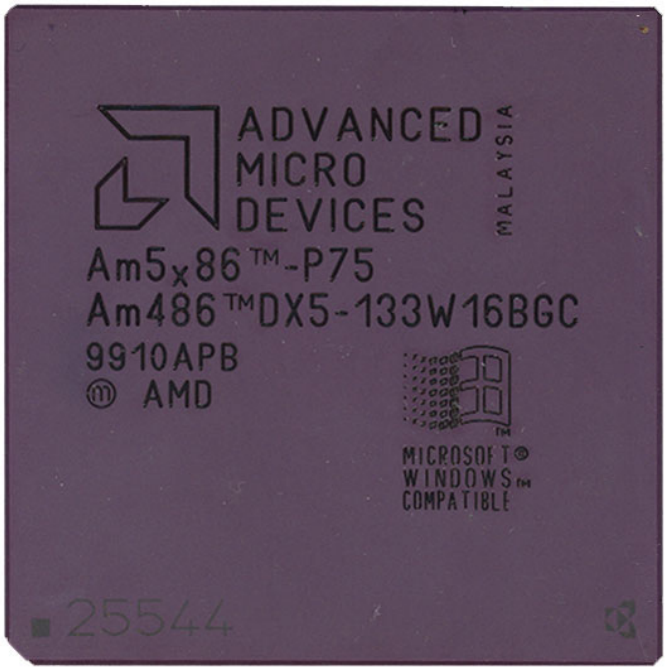




IBM-marked 5x86C CPUs tend to over-clock better, especially to 133 MHz, and at lower voltages compared to Cyrix-marked pieces, especially those CPUs with a QFP package, as shown below.



Cyrix-marked CPUs with a 1996 date code may over-clock better than ones with a 1995 date code since Cyrix was focusing on 133 MHz chips in early 1996. The last batch of Cyrix 5x86 CPUs had a date code of Week 7, 1996. Cyrix 5x86-133 CPUs have been thoroughly tested on this motherboard for stability and performance. The Cyrix 5x86-133 is considered by many as the fastest stock socket 3 CPU available; it equals or surpasses an over-clocked Pentium Overdrive 100 MHz CPU in arithmetic logic functions even though the POD100 is superscalar and incorporates a pipelined parallel ALU execution path. The overclocked Am5x86-160 and POD100 have similar ALU performance to that of the [non-overclocked] Cyrix 5x86-133/4x. One of the later production (1999) Am5x86 chips is shown below alongside the Cyrix 5x86-133. Unfortunately, not even an Am5x86 chip with this late of a production date would function reliably at 180 MHz, even with voltages up to 4 V. For a comparison of 486 CPUs benchmarked on a Um8881-based socket 3 motherboard, refer to the following weblink,
http://www.vogons.org/viewtopic.php?t=28470



For IBM and Cyrix 5x86 processors, Load/Store Reordering (LSSER), Memory Read Bypassing (MEM_BYP), Fast FPU Exception Handling (FP_FAST), Linear Burst Cycles (LINBRST), Burst Write-Back Cycles (BWRT), Speculative Execution of RET Instructions (RSTK_EN), Prefetch Buffer Loop (LOOP_EN), and Directory Table Entry Cache (DTE_EN) all work with this CPU/motherboard pair in DOS, Windows 9x, Windows NT, and Windows 2000. Branch Prediction (BTB_EN) works reliably in DOS only for Stepping 0, Revision 5 CPUs, while Stepping 1, Revision 3 CPUs are reported to work well within DOS and Windows. If enabling BTB, you must disable LOOP and sometimes RSTK in, both, DOS and Windows. Further information on the performance benefit of each Cyrix 5x86 register setting can be found by reading the following weblinks,
http://www.vogons.org/viewtopic.php?t=30607
http://www.vogons.org/viewtopic.php?t=45756

For **DOS**, I use the Peter Moss utility to enable Cyrix features with the following settings,

Stepping 0, Revision 5

```
5x86.exe /LSSER=off /FP_FAST=on /BWRT=on /LOOP_EN=off /RSTK_EN=on /BTB_EN=on
```

Stepping 1, Revision 3

```
5x86.exe /LSSER=off /FP_FAST=on /BWRT=off /LOOP_EN=off /RSTK_EN=off /BTB_EN=on
```

Note that MEM_BYP, DTE_EN, LINBRST, and L1 write-back cache are enabled by default on this motherboard and do not need to be software enabled like on some other motherboards. S1R3 CPUs do not support BWRT. If overclocking S1R3 CPUs to 120 MHz, there are reports that LSSER might need to be set ON (=1), which is not optimal. LSSER, FP_FAST, and BTB have the largest impact on performance.

For **Windows 95/98/98SE**, I also use the Peter Moss utility with the following settings,

Stepping 0, Revision 5

5x86.exe /LSSER=off /FP_FAST=on /BWRT=on /LOOP_EN=on /RSTK_EN=on /BTB_EN=off

Stepping 1, Revision 3

5x86.exe /LSSER=off /FP_FAST=on /BWRT=off /LOOP_EN=off /RSTK_EN=off /BTB_EN=on

For **Windows NT 4.0** and **Windows 2000**, you must use the Evergreen 5x86 utility, which loads a driver, ET586NT.SYS, into your Control Panel/Devices folder, and is set to run at System boot. The values this program requires are in decimal, however the same values stored in HKEY_LOCAL_MACHINE\SYSTEM\ControlSet001\Services\ET586NT\Parameters are converted to and stored in HEX.

Stepping 0, Revision 5

Cache Mode: Write Back Cache

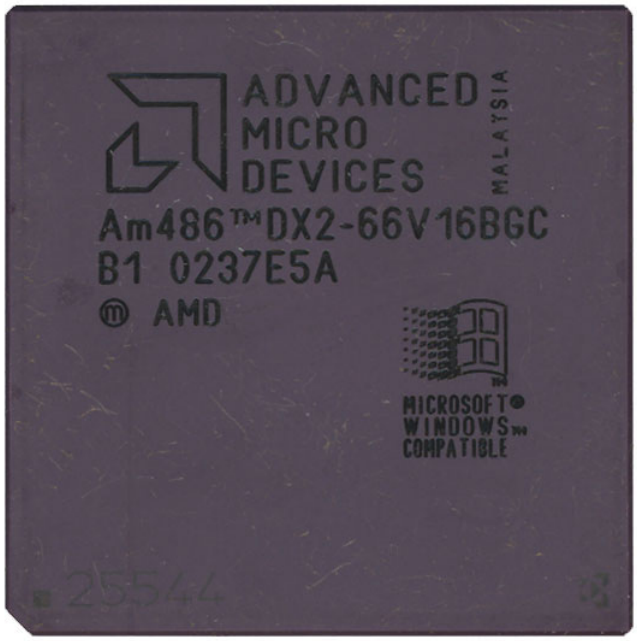
Set Startup Type: Yes, attempt to setup
PCR0 = 5
CCR1 = 2
CCR2 = 214
CCR3 = 28
CCR4 = 56

Stepping 1, Revision 3

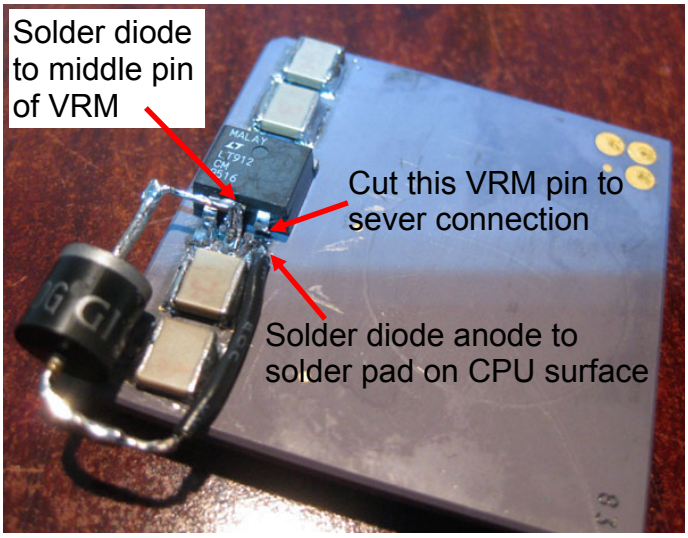
Cache Mode: Write Back Cache

Set Startup Type: Yes, attempt to setup
PCR0 = 2
CCR1 = 2
CCR2 = 150
CCR3 = 28
CCR4 = 56

There have not been any reports of successful testing with the 83 MHz FSB setting. Since the multiplier request setting on 486 motherboards is only 1-bit, it allows for only 2 discrete multiplier requests, namely 4×/2× and 3×/1×, with the variable being CPU-determined. While many AMD Am5x86-133 chips can be over-clocked to 160 MHz and sometimes to 180 MHz, they interpret a 2× request as a 4× request and will not run at 2×83 MHz. Am5x86 CPUs only multiply the FSB by 3× or 4×. The only CPUs which might work at 2×83 (166 MHz) are an AMD DX4-120SV8B with a mid-1996 date code or an Am486 DX2-66V16BGC with a 1998+ date code. The later is likely an Am5x86 chip with the multiplier option set to 2× and 3×. An Am486 DX2-66V16BGC was acquired for testing and although the system was able to boot at 2x83, it was not stable. 3dbench was able to run but there were artifacts on the screen. The chip ran well at 2x66 MHz though.

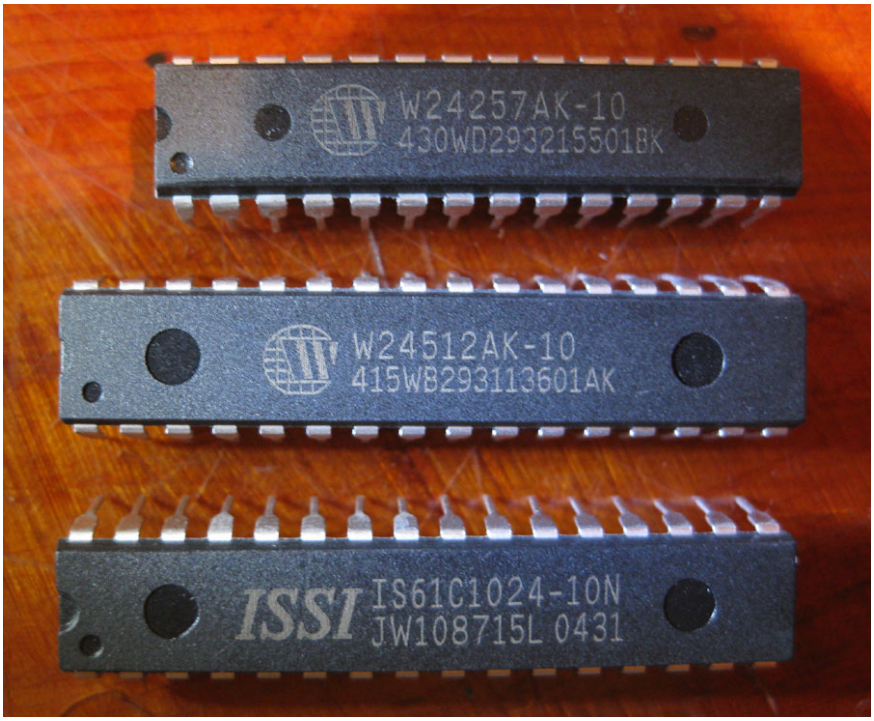


Some Pentium Overdrive 83 (POD83) units will run stable at 100 MHz off the shelf, however this is not common. The POD has an onboard voltage regulator which drops the voltage down to 3.3 V. This also means you cannot increase the POD's operating voltage without some modification. One can cut the lead which sends 3.3 V to the CPU and modify the incoming 5 V lead to run at 4 V by adding a 4-6 ampere diode. 4 V is usually sufficient to run the CPU at 100 MHz.
More information can be found from this weblink, http://www.vogons.org/viewtopic.php?p=457441



Level 2 Cache

The MB-8433UUD has 9 sockets for SRAM cache, 5 DIP-28 and 4 DIP-32. The DIPs can accept up to 512 KB of single-banked L2 cache using 4 DIP-32 sockets (each chip is 128 Kbyte, or 1024 Kbit [128 Kbit × 8]), or up to 256 KB of double-banked cache using 8 DIP-28 sockets [32 Kbit × 8, each module]. Some 10 ns cache examples are shown below.



32 Kbit x 8
DIP-28

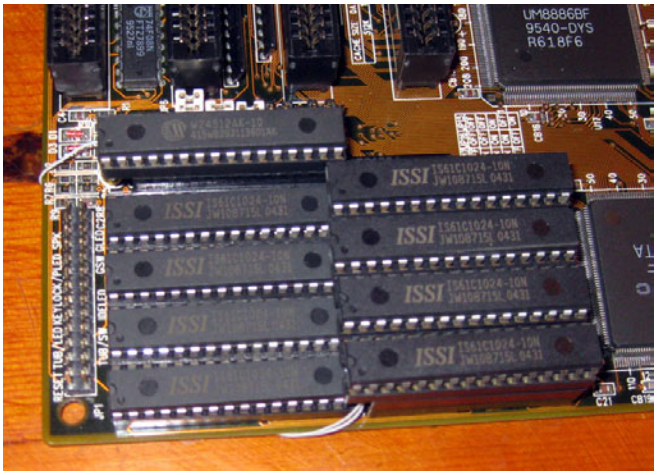
64 Kbit x 8
DIP-32

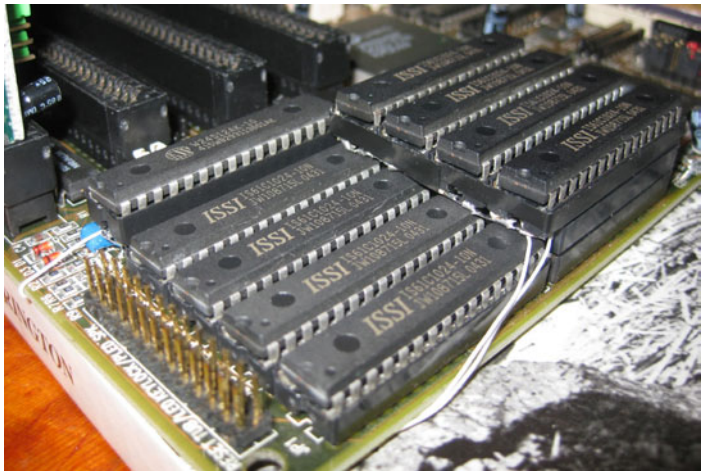
128 Kbit x 8
DIP-32

Double-banked 256 KB cache can run stable with faster cache timings compared to 512 KB single-banked cache when using FSB's at 40 MHz or higher. It is not clear why the board manufacturer, Biostar, did not implement all cache sockets as DIP-32 as this would accommodate 1024 KB of double-banked cache. The UMC 8881 chipset supports bank interleaving when both cache banks are filled. The TAG RAM in both cases is a single DIP-28 256 Kbit piece. When using 512 KB of WB cache, the cacheable memory range is limited to 64 MB, and with the cache in WT mode, the cacheable memory range is extended to 128 MB. The performance drop associated with write-through L2 cache compared to write-back L2 cache was observed to be less than 5%. Note that installing more memory than can be cached results in an ~30% performance drop in Windows (DOS is unaffected). Most users will find little benefit in increasing the RAM from 64 MB to 128 MB unless they are using a web browser. The original BIOS did not have the option to set the L2 cache into write-through mode, however this was later modified by the author using Modbin. When running the system with tight cache timings, or when overclocking the bus, I found it best to use 256 KB of double-banked cache. If running the FSB at 60 or 66 MHz, it is best to have cache rated at 10 or 12 ns.

The main downfall of the MB-8433UUD is that the L2 cache size is limited to a single bank of 512 KB, or double-banked 256 KB. While the UMC chipset adopted on this motherboard supports 1024 KB of cache, a modification to the motherboard's PCB is required for this to work. After some rewiring work, 1024 KB cache operation was realised on this motherboard, however the fastest stable cache timing was 3-1-1-1 at 33 MHz FSB with 128 MB RAM, or 3-2-2-2 at 66 MHz FSB with 128 MB RAM. Normally, 2-1-1-1 runs stable at 33 MHz with 256-512 KB of L2 cache. I do not recall if 64 MB was stable at 2-1-1-1 at 33 MHz FSB w/1024K - my notes indicate that it passed MemTest. 1024 KB of cache allows for fully cached 128 MB of RAM in write-back mode, or 256 MB of RAM in write-through mode. In addition to the increase in cacheable range for system memory, there is some general performance gain due to an increase in cache hits associated with more cache. CPUMark99 benchmarks revealed an increase in performance when going from 256K to 512K at 3.6% and from 256K to 1024K at 9.4%. This gain seems a bit exaggerated for real-world applications. I suspect the real benefit is closer to 1-2%.

Below are images of a MB-8433UUD which has been modified to accept 1024K L2 cache.



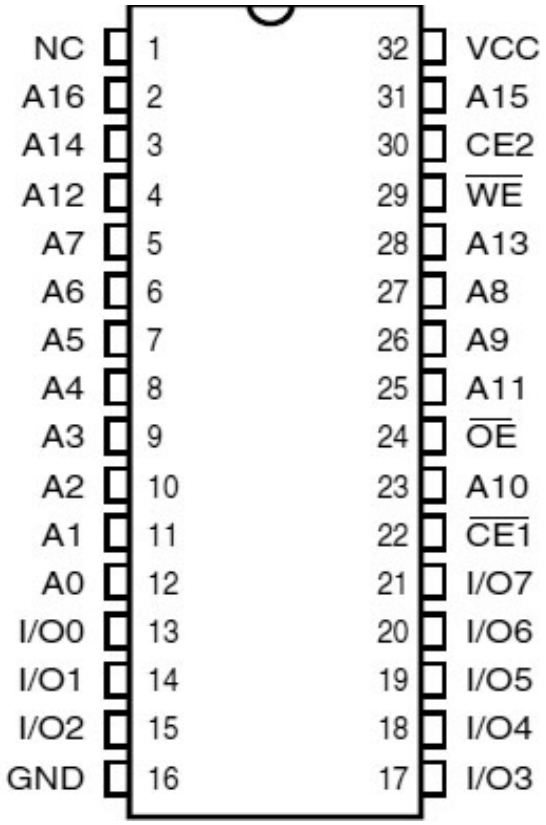


The details of the 1024K modification are as follows,

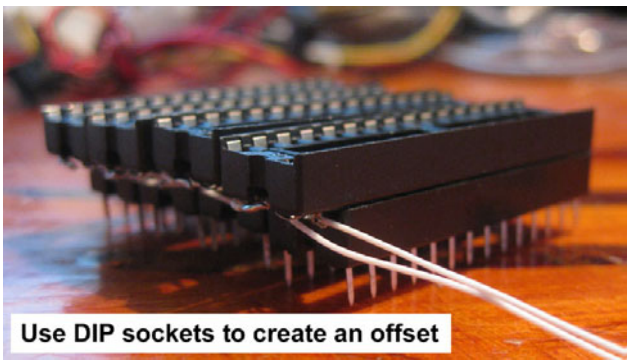
1) Gang up (solder together) all CACHE A15 pins on the 4 extension DIP-32 sockets and wire to CACHE A15 on the other, existing, DIP-32 bank. See photos below.
2) 2) Gang up all CACHE A16 pins on the 4 extension DIP-32's and wire to CACHE A16 on the other, existing, DIP-32 bank.
3) Wire CE2 (cache pin 30) on extension DIP-32's to Vcc for both CACHE and TAG extensions. Wire Vcc (pin-32) to Vcc, e.g. to CE2.
4) Solder in a 10K SMD resistor between TAG A16 and Vcc on TAG DIP-32 extension
5) Solder in a 10K SMD resistor between TAG A15 and Vcc on TAG DIP-32 extension
6) Wire TAG A15 and CACHE A16 to Um8881 pin 20. Refer to accompanying photos below. This is easily accomplished by soldering TAG A15 and CACHE A16 to JP6-pin4 and to CPU pin A19.
7) Wire N/C pins of TAG and CACHE extensions to Vcc
8) Replace the 10 uF capacitor under the TAG DIP-32 extension with a shorter capacitor. You can also solder the capacitor onto the underside of the board.
9) Set jumper JP6 to 1-2, 3-4 and JP5 to 2-3 and JP7 to 2-3.

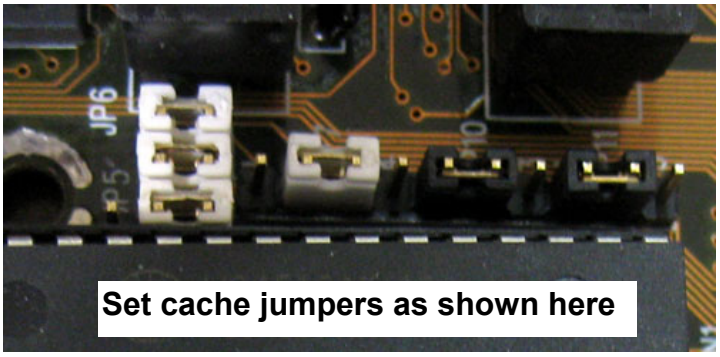
These are the unjumpered pin assignments for the cache jumpers which are useful for those wanting to determine the modifications required 512 KB double-banked cache. While I have confirmed a modification for 512 KB double-banked cache also works, I did not make note of the hardware configuration required. I recall there was little difference between 1024K and 512K double-banked, perhaps just the TAG wiring.

	Pin	Connected to:
JP5	1	Um8881 pin 62 and CACHE Bank0 A11
	2	CACHE Bank1 A10
	3	Um8881 pin 22 and CACHE Bank0 A10
	Pin	**Connected to:**
JP6	1	Um8881 pin 22 and CACHE Bank0 A10
	2	TAG A13
	3	Um8881 pin 21
	4	TAG A14
	Pin	**Connected to:**
JP7	1	Um8881 pin 22 and CACHE Bank0 A10
	2	CACHE Bank1 A15
	3	Um8881 pin 21
	4	CACHE Bank1 A16

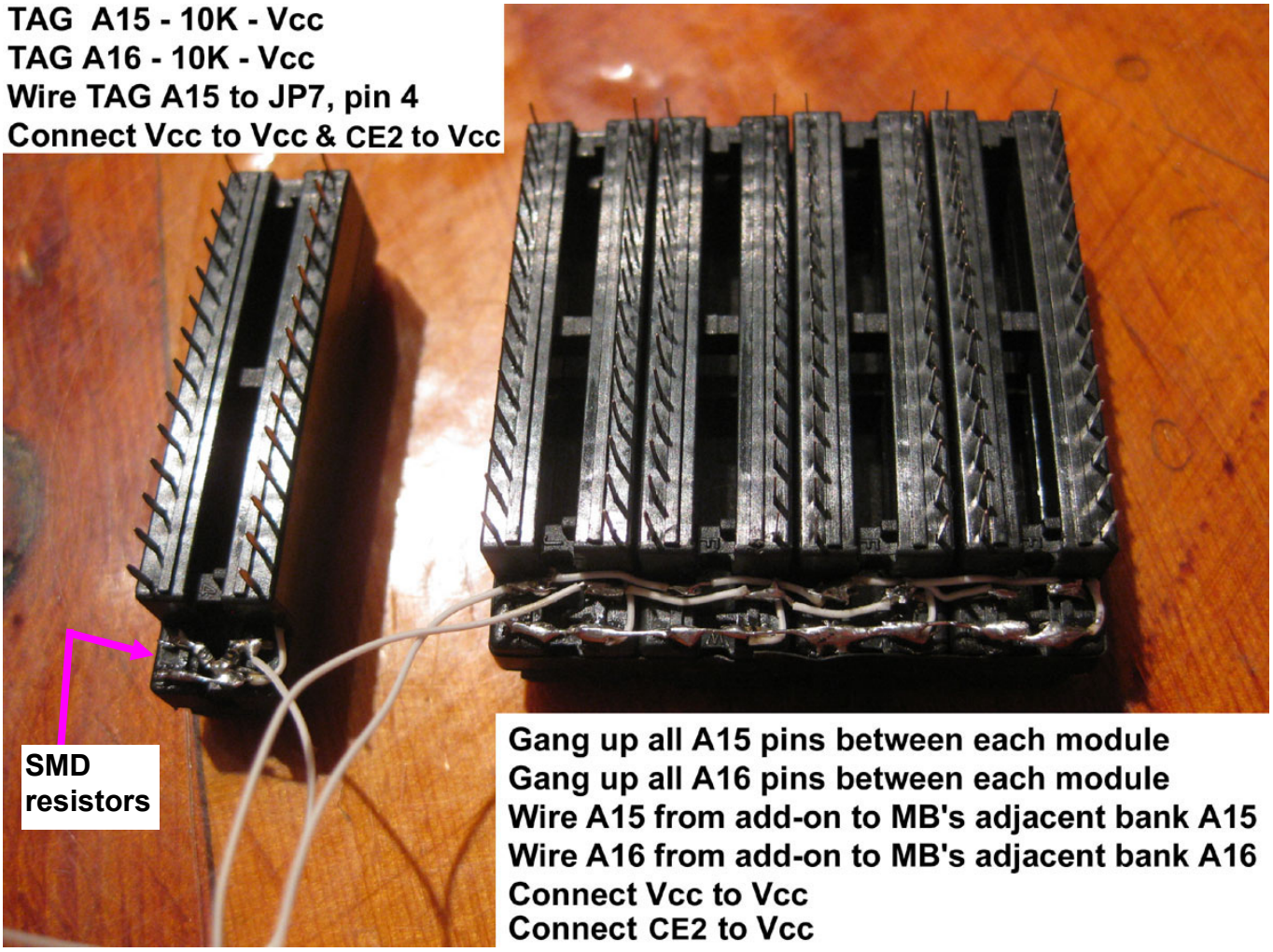


DIP-32 pin assignments

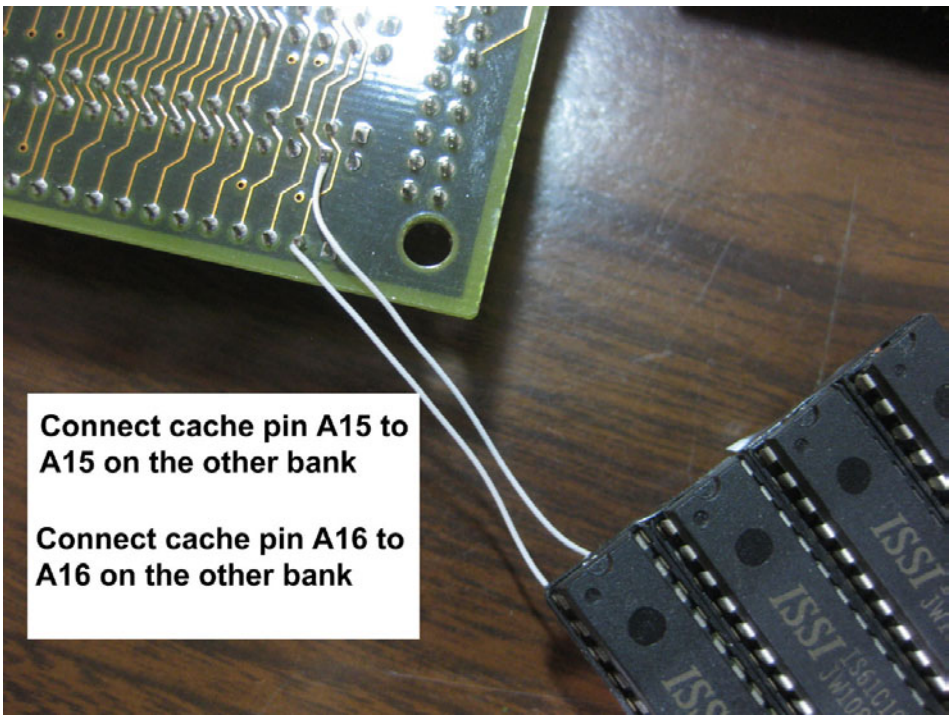


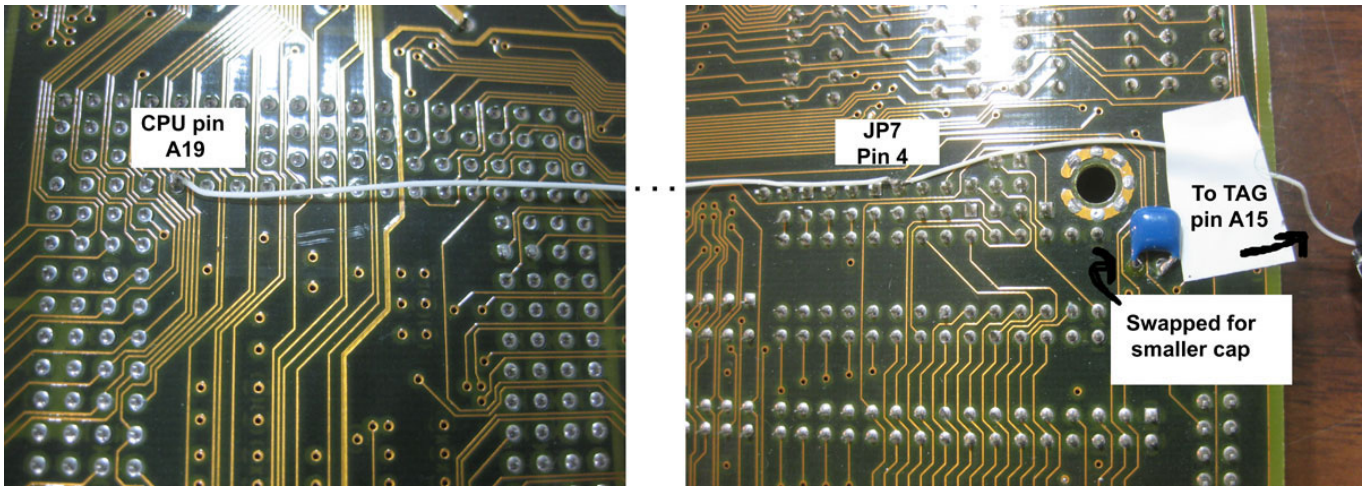


TAG A15 - 10K - Vcc
TAG A16 - 10K - Vcc
Wire TAG A15 to JP7, pin 4
Connect Vcc to Vcc & CE2 to Vcc



Gang up all A15 pins between each module
Gang up all A16 pins between each module
Wire A15 from add-on to MB's adjacent bank A15
Wire A16 from add-on to MB's adjacent bank A16
Connect Vcc to Vcc
Connect CE2 to Vcc





Expansion

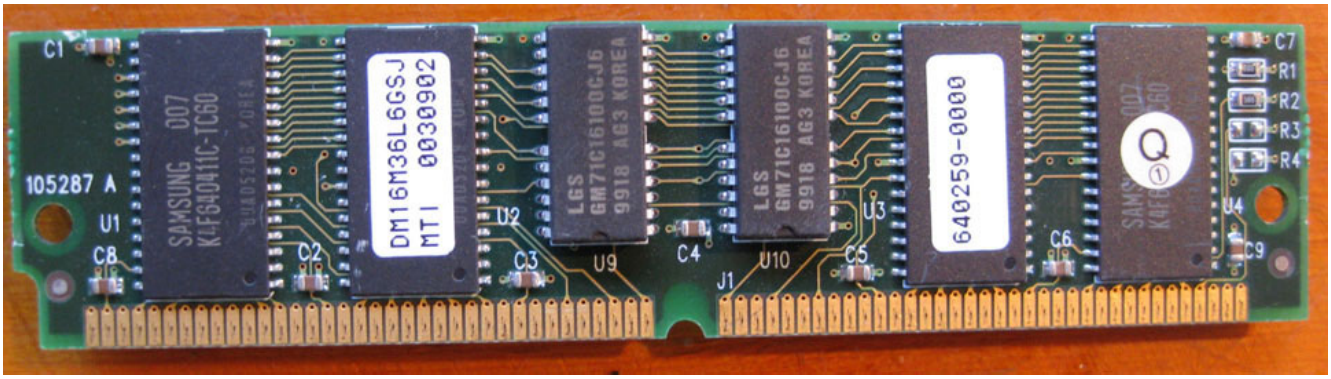
The board has four 8 MHz ISA slots and three 33 MHz PCI slots with room between them so they're not shared like on some motherboards. It is not well documented which revision of PCI is supported by this motherboard, but it is likely either PCI 2.0 or PCI 2.1. PCI 2.0 emerged on April 30, 1993 (5 V only), while PCI 2.1 emerged on June 1, 1995 (5 V and 3.3 V). The maximum throughput of the PCI port is 133 MB/s, or 33.3 MHz × 32 bits / (8 bits / byte). This motherboard properly supports SCSI bus mastering, which is hard to find on a socket 3 motherboard. A good test for proper functionality is to install and boot Windows 2000 with an Adaptec PCI SCSI card. If your hard-drive gets hung-up in an infinite loop of access attempts, chances are you have SCSI bus mastering problems. The HOT-433 and M919 both have issues with this, even though they both use the same chipset as the MB-8433UUD. The HOT-433 and M919 will also sometimes exhibit SCSI bus mastering issues in Windows NT 4.0 and Windows 98SE, but the occurrence is infrequent.

Chipset

The MB-8433UUD uses the UMC 8881/8886 series of chipsets. The newest date codes encountered for the UMC chipset were UM8886BF (9703-FXA) and UM8881F (9651-EYA), found on an M919 motherboard. UM8881F is the Northbridge (memory controller) and UM8886BF is the Southbridge. It was noted online somewhere that the *E* in 9651-*E*YA may be required for proper EDO support.

Memory

The MB-8433UUD has four 72-pin SIMM sockets and supports EDO RAM with the UUD960326i or newer BIOS. Pantex Computer's Tech Base reports that TI memory doesn't work with the MB-8433UUD. The Northbridge Cache/Memory controller, UM8881F, supports up to 256 MB of either EDO or FPM memory. Fast-Page Mode memory (FPM) seems to be the fastest and most reliable on this motherboard. EDO RAM will also work but the cache timing may need to be reduced to 3-2-2-2 at 40 MHz FSB, or 3-1-1-1 with a 33 MHz FSB. Samsung FPM memory with module markings of K4F640411C-TC60 seem to work best for over-clocking. 256 MB of RAM tested good using MemTest v4.0 and is stable in Windows, however only 64 MB (of the 256 MB) was cacheable with 512 KB WB cache during this test. The BIOS was modified to allow for setting the L2 cache into write-through mode and will cache 128 MB in write-through mode. When running the system with tight cache timings, or when overclocking the bus, it is best to use a single stick of FPM memory (32 MB or 64 MB). The following CMOS Dynamic Fast-page Mode w/Parity stick works particularly well on this motherboard when overclocking. It is 64 MB, 72-pin, 5 V, and 60 ns.



Graphics

The following weblink lists all the higher-end PCI graphics cards and driver revisions I have tested on this motherboard. http://www.vogons.org/viewtopic.php?t=33879

My favourite combination is using a Matrox Millennium G200 with a Voodoo2 or a Nitro 3D (S3 Virge GX - 86C385) with a Voodoo2. Unfortunately, Voodoo Banshee and Voodoo3 cards do not work with UMC 8881 chipsets; although they work with some SiS 496/497 chipsets. For Win9x, the latest working Matrox G200 driver version is 4.33c. For WinNT 4.0, the latest working Matrox driver version is 5.06. With version 5.06, OpenGL is correctly implemented. OpenGL with the Win9x driver does not work, but Direct3D does work.

Communication Ports

The board contains one UMC 8663BF chip and one 8667 chip. The 8667 chip contains two 16550 UART serial ports, while the 8663 contains a SPP/EPP/ECP-DMA parallel port and a floppy controller.

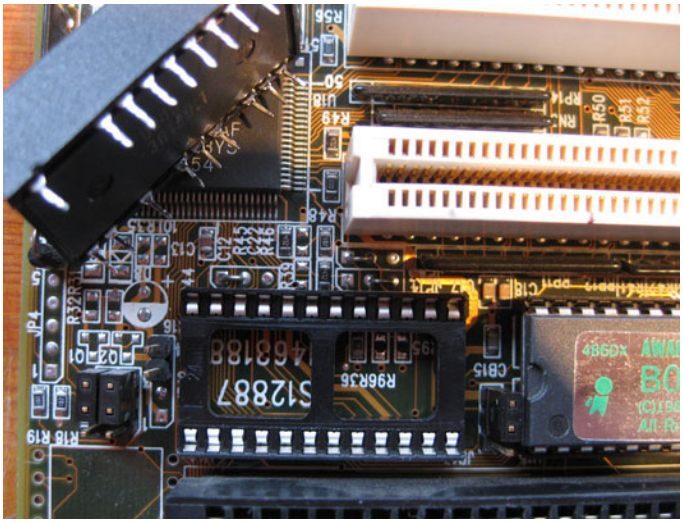
IDE Storage

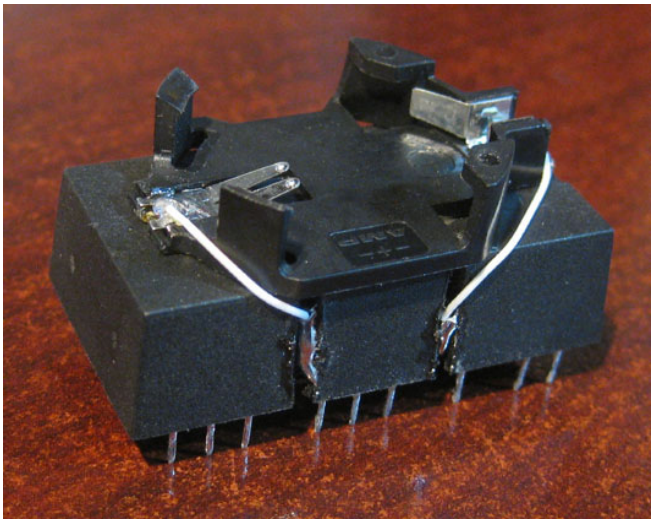
There are built-in primary and secondary Enhanced IDE controllers capable of PIO-4 speeds contained within the UM8886 chipset. According to the BIOS, the hard disk controller will do PIO modes 1 through 4. For Linux, OS/2, and other real multitasking OS users, the MB-8433UUD does not use the buggy RZ1000 or CMD640B IDE controller chips. Some have reported issues with the EIDE driver and Novel Client 32 when using the UM8673.sys driver. I have not been able to locate a working DMA driver for the IDE port. When I use the UMC-supplied IDE driver, Win9x becomes unresponsive. Stick with the Windows-supplied drivers. If you are using a CF card, set the IDE Primary Master PIO to PIO-4 instead of AUTO. I have experienced problems when booting to a CF card if AUTO is set.

Real-time clock (RTC)

While the PCB layout has solder pads to accommodate a regular CMOS battery, I have not come across any boards which do not have the ODIN/DALLAS real-time clock (RTC) module with integrated battery. Version 3.0/3.1 boards often came with a socketed RTC chip, which can be replaced easily when the internal battery dies, otherwise, desoldering of the RTC is required. The typical Dallas battery lifespan is 15 years. Speedsys reports that Dallas RTC's with model DS12887A have the Y2K bug, whereas models marked DS12887 do not. I'm not sure if this matters at all or if Speedsys is conveying true information. It is important that you obtain a RTC module with an 'A' suffix because these allow for clearing the CMOS data with the JP12 jumper. Boards without the 'A' suffix cannot clear CMOS data.

These motherboards are at the age in which all the onboard RTC modules will have dead or nearly dead batteries. If your RTC is soldered onto the board, you will want to desolder it and replace it with a DIP-22 socket, as shown below. You will then need to purchase a new DALLAS RTC module to insert into the socket, or modify your old RTC to include a CR2032 battery holder. The latter is accomplished by cutting away the plastic at pins 16 and 20 and soldering on 2 wires which connect to the battery holder. Pin 20 is for the positive lead, while pin 16 is for the negative lead. An example of this modification is shown below. Although this modification allows for two batteries of different potential being connected in parallel, it seems to work none-the-less.





Keyboard/Mouse

The board is complete with an AT-style keyboard and PS/2 mouse port (and header). The Southbridge (UM8886BF) is responsible for keyboard and PS/2 mouse implementations, whereas some older 486-era motherboards employed a specific i8042-class keyboard controller chip. You can easily create your own PS/2 mouse cable; the pin-outs are provided later in the manual.

Some users reported Windows 95 having issues with the PS/2 mouse, however none of the boards tested herein had issues. This is an excerpt from one user,

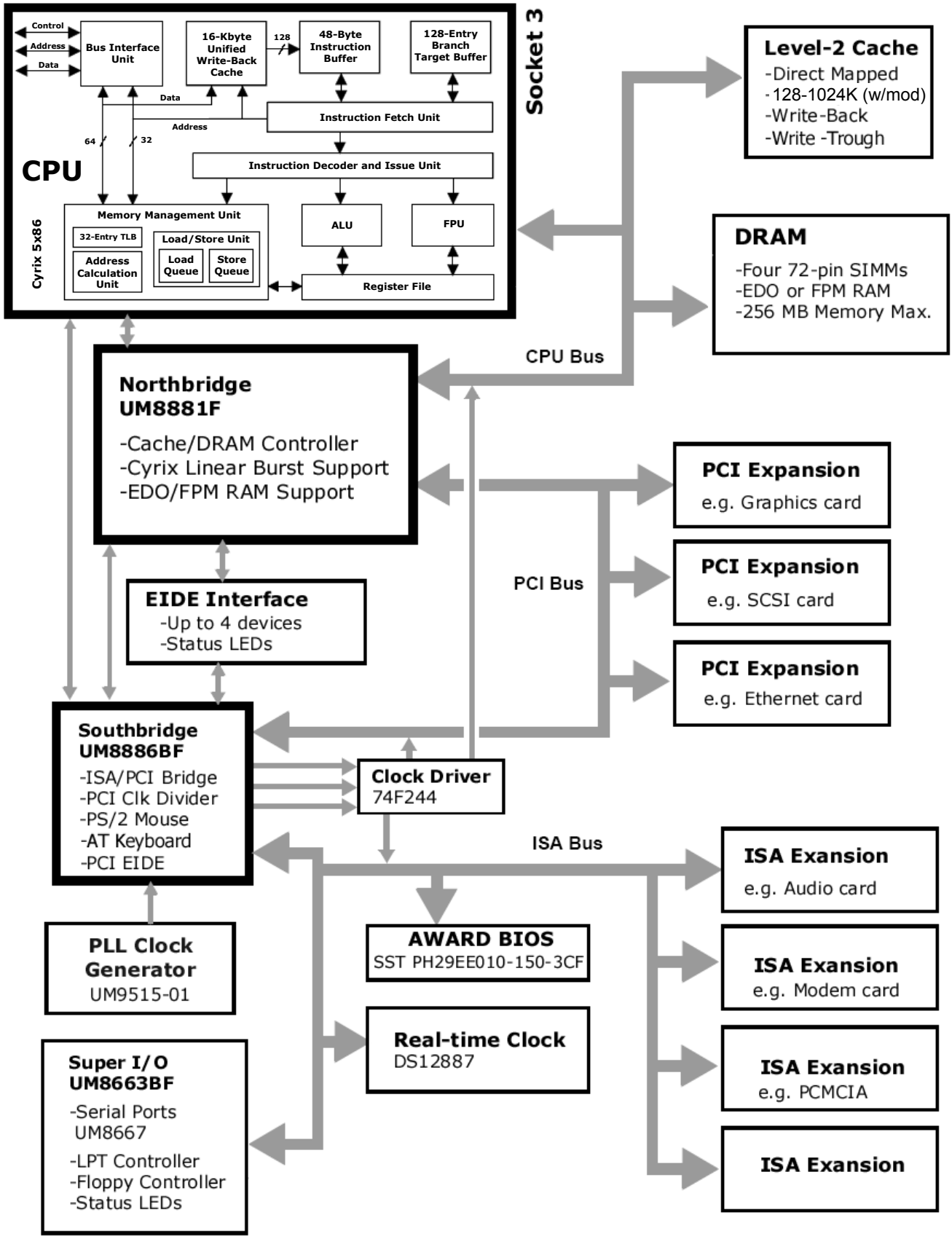
> *Under Windows 95, the keyboard and PS/2 mouse may conflict causing a complete loss of control. If you press a key, a mouse button, and move the mouse at the same time, both the keyboard and mouse become unusable. If you then warm-boot the machine, it will "update ESCD" and remove PS/2 mouse support! You will need to cold-boot to get the mouse back. Without mouse or keyboard, you can't shut down Windows properly. The problem was repeatable in Windows 95's real mode (DOS prompt), under DOS 6.22, and in Linux under XFree86, so it's not just a Windows 95 driver issue. Quantex reports this problem as unresolved on their page of support info. They say it's a bug in the UMC I/O controllers, and I believe it. This problem can be worked around by simply using a serial mouse instead of a PS/2 mouse. I'm running fine with an old Logitech mouse on COM2 right now.*

The only mouse-related issues I have experience occurs just after booting Windows 95. If I move the mouse around just after boot and while the HDD hasn't finished all boot activity, the system may hang. Once the system is fully booted, however, the problem is non-existent. I did not experience the same issue with Windows 98SE or Windows NT 4.0.

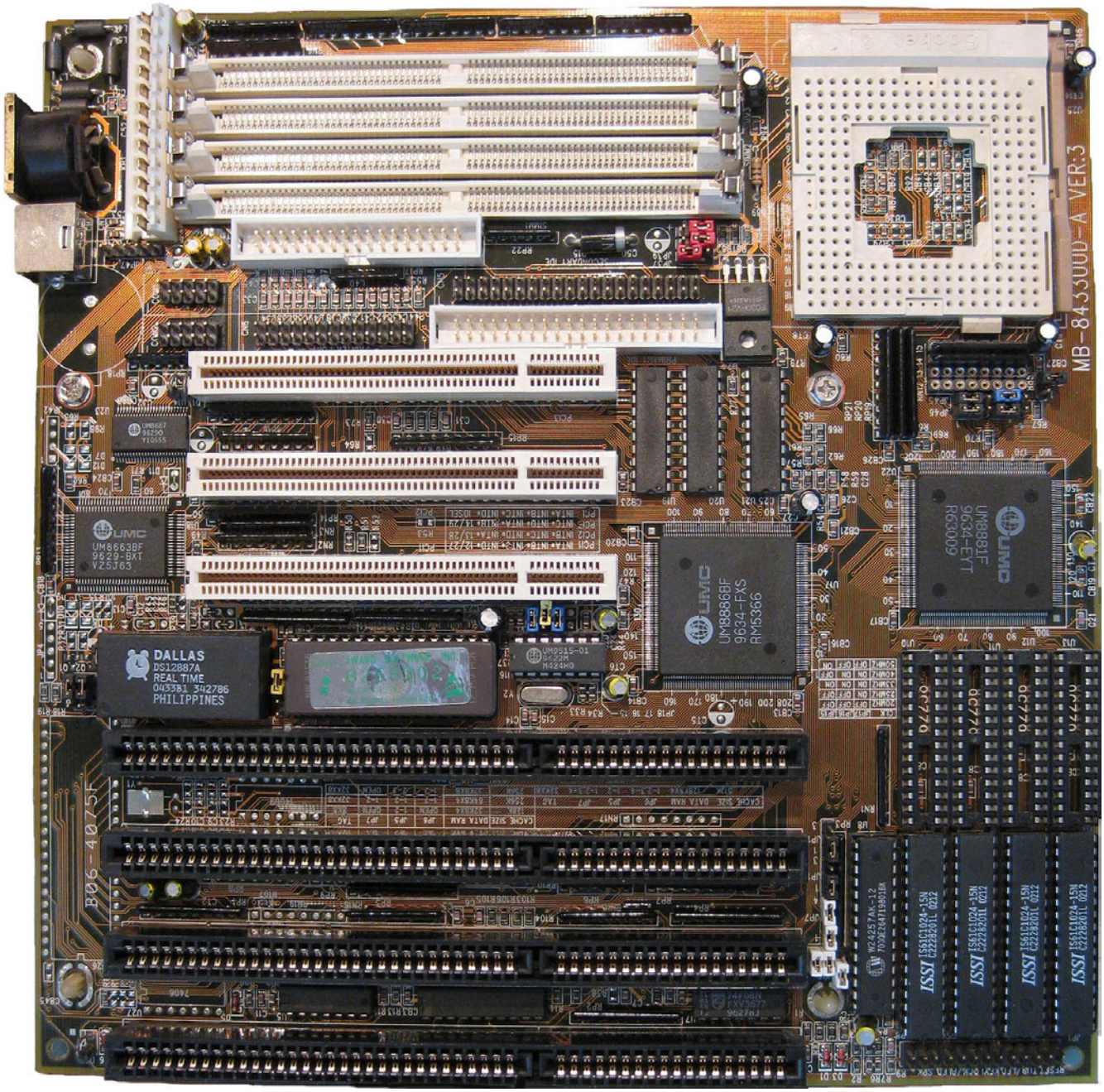
Hardware Compatibility List (incomplete)

Adaptec AHA-2940U2W SCSI
Adaptec 19160 Ultra160 SCSI
Matrox Millennium G200
Matrox Mystique 220
Voodoo2
Diamond V550 RIVA TNT
GeForce2 MX400
STB Nitro3D S3 VirgeGX
S3 Trio3D
S3 VirgeDX
S3 Trio64
ATI Rage 128 VR
AWE64 Gold, CT4390
AWE64 Value, CT4500
Audican32 Plus
3Com 3c905C-TX-M
3Com 3c515-TX ISA
3Com 3c509B-TPO
Intel Pro 100S
Intel EtherExpress Pro 100 ISA
Brother HL-5250DN
U.S. Robotics 5687 v.90 56K ISA modem
USB Host Controller, SIIG Intek 21 (TKP2U022) OPTi 82C861
Creative DXR2 DVD/MPEG Decoder
Promise SATA150 TX2plus
Promise Ultra100 TX2
ACARD AEC7732U Bridge Adapter
ACARD AEC7720U Bridge Adapter
Logitech 3-button PS/2 MouseMan, M-S38
Logitech 3-button PS/2 optical mouse with scroll wheel, M-SBF96

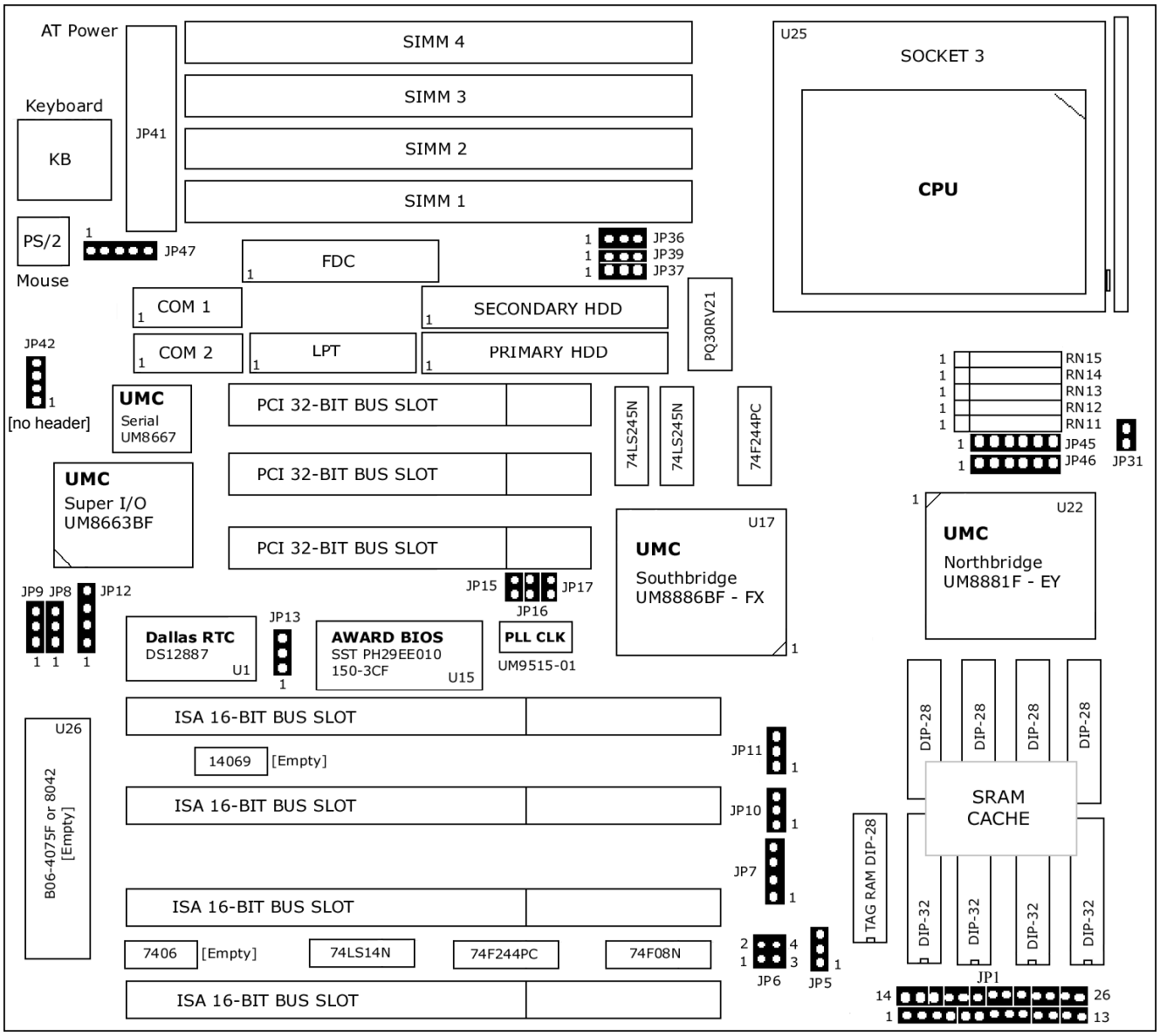
Functional Block Diagram



Motherboard Photo (unmodified)



Board Layout and Jumper Locations



74LS14N is a HEX Shmitt-trigger inverter.
74F244PC is a line driver (buffer) for the ISA/PCI/CPU clocks.
74F08N is a 4-input AND gate.
74LS245N is a bus transceiver for communication between different buses.
PQ30RV21 is the CPU core voltage regulator (Sharp).
UM9515-01 is the Phase-Lock Loop (PLL) circuit which derives all the possible FSB frequencies from single 14.3 MHz crystal oscillator.

Mouse Data goes to pin 199 of UM8886BF.

Mouse Clock goes to pin 200 of UM8886BF.

Keyboard Data goes to pin 56 of UM8886BF.

Keyboard Clock goes to pin 57 of UM8886BF.

Jumper Settings

JP1 – External Connectors	**JP16** – CPU Clock Select
JP5, **JP6**, **JP7** – Cache RAM Size Select	**JP37**, **JP39** – CPU Voltage Select
JP8, **JP9** – ECP DMA Channel Select	**JP12** – CMOS Discharge for boards w/ Dallas or ODIN RTC module **JP42** – CMOS Discharge for boards w/external battery (uncommon)
JP13 – BIOS ROM Type Select	**JP10, JP11**, **JP31**, **JP45**, **JP46**, **RN11-RN15** – CPU Type Select

Connectors – JP1

Pin	14	15	16	17	18	19	20	21	22	23	24	25	26
Signal	+	-	N/C	CTR	Gnd	N/C	-	+	N/C	CTR	Gnd	Vcc	Gnd
Connector	Green LED		N/C	Green Switch		N/C	HDD LED		N/C	Turbo* Switch			

Pin	1	2	3	4	5	6	7	8	9	10	11	12	13
Signal	CTR	N/C	Gnd	Vcc	+	N/C	Gnd	CTR	Gnd	-	+	CTR	Gnd
Connector	+	Speaker		-	Power LED			Key Lock		Turbo LED		Reset SW	

*The motherboard is in turbo mode when pins 23-24 are open. Turbo is disabled when pins 23-24 are shorted. Shorting pins 23-24 adds extra wait states, or clock cycles, to the Level-2 cache and RAM, lowering bandwidth by about 5×.

ECP DMA Channel Select – JP8, JP9

DMA Channel	JP8	JP9
1	1-2	1-2
3	2-3	2-3

ROM Type Select – JP13

ROM Type	JP13
SST (+5V) EEPROM	1-2
Intel (+12V) EEPROM	2-3
UV EPROM	open

CMOS Discharge – for Dallas RTC DS12887A(BQ3287A) and ODIN OEC12C887A – JP12*

Function	JP12
Normal Operation	open
Discharge	3-4

*RTC modules with the 'A' suffix must be used if you wish to discharge CMOS data

CMOS Discharge – for boards with external battery (uncommon) – JP42*

Function	JP13
Normal	2-3
Discharge	3-4

*An external 4.6V battery may also be attached to JP42. Attach the positive wire (+) to pin 1 and the negative wire (-) to pin 4. Most boards only have solder pads for JP42.

Asynchronous SRAM Cache Size Select – JP5, JP6, JP7

Total SRAM Size	SRAM Configuration (each piece)	SRAM Example (part number)	TAG RAM Configuration (1 piece)	Cacheable Range **Write-back**	Cacheable Range **Write-thru**	JP5	JP6	JP7
128 Kbyte 4 pieces	32 Kbit × 8	W24257AK-15	8 Kbit x 8	16 Mbyte	32 Mbyte	1-2	open	open
256 Kbyte 4 pieces	64 Kbit × 8	W24512AK-15	32 Kbit x 8	32 Mbyte	64 Mbyte	1-2	1-2	1-2
256 Kbyte 8 pieces ‡	32 Kbit × 8	W24257AK-15	32 Kbit x 8	32 Mbyte	64 Mbyte	2-3	1-2	open
512 Kbyte 4 pieces	128 Kbit × 8	IS61C1024-15	32 Kbit x 8	64 Mbyte	128 Mbyte	1-2	1-2, 3-4	1-2, 3-4
512 Kbyte 8 pieces +	64 Kbit × 8	W24512AK-15	32 Kbit x 8	64 Mbyte	128 Mbyte			
1024 Kbyte 8 pieces +	128 Kbit × 8	IS61C1024-15	64 Kbit x 8	128 Mbyte	256 Mbyte	2-3	1-2, 3-4	2-3

‡ 8 pieces of cache constitutes two banks; 4 pieces is a single bank. Two banks are required for the chipset to interleave the cache. Double-banked cache can usually handle faster cache timings compared to single-banked cache.

+ Additional hardware modification required. Modification details can be found elsewhere in this manual.

Front-side Bus (FSB) Clock Selection – JP15, JP16, JP17

FSB Clock	JP15	JP16	JP17*	FSB Clk : PCI Clk
20 MHz	open	open	open	1:1
25 MHz	open	open	closed	1:1
33 MHz	closed	closed	closed	1:1
40 MHz	open	closed	closed	1:1 if stable, otherwise 1:2/3
50 MHz	closed	open	open	1:2/3
60 MHz	open	closed	open	1:1/2
66 MHz	closed	open	closed	1:1/2
83 MHz	closed	closed	open	1:1/2 if lucky

*JP17 exists only on some motherboards, otherwise it is soldered closed. It can be unsoldered and replaced with a jumper header. Version 1 and some older version 2.0 boards have JP17 soldered closed.

§ Clocking your chipset and related components above specification may cause component damage.

CPU Multiplier Selection – JP45

CPU Multiplier	JP45
1x	1-2 or 2-3
2x	1-2, 4-5
3x	1-2
4x	1-2, 4-5

CPU Voltage Selection – JP37, JP39, JP36

CPU Voltage	JP37	JP39	JP36
3.45 V	2-3	2-3	2-3
4 V* or 3 – 4 V variable	1-2	2-3	2-3
5 V	2-3	1-2	1-2

*The SMD resistor, R82, can be removed and a 5 K-ohm variable resistor (trimmer) put in its place, allowing for the 4 V setting to output CPU voltages ranging from 3.0 V to 4.1 V with mV tuning.

CPU Type Selection – JP10, JP11, JP31, JP45, JP46, RN11-RN15

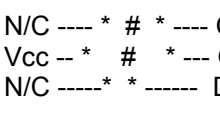
CPU Type	JP10	JP11	JP31	JP45	JP46	RN11	RN12	RN13	RN14	RN15
Intel 486 DX/DX2	1-2	1-2	open	2-3	1-2, 4-5	open	open	open	close	close
AMD 486 DX2 NV8T	1-2	1-2	open	2-3, 5-6	1-2, 4-5	open	open	open	close	close
AMD 486 DX4 NV8T	1-2	1-2	open	2-3	1-2, 4-5	open	open	open	close	close
Intel P24D DX2/DX4 (WB) Intel P24C DX2/DX4 (WT) AMD Enhanced DX/DX2/DX4 AMD 486 SV8B, SV16B, SV8T Cyrix 5x86 M1SC [M9] AMD Am5x86 / X5	1-2	1-2	open	1/3x : 1-2 2/4x : 1-2, 4-5	1-2, 4-5	open	open	open	close	close
Intel Pentium Overdrive P24T	1-2	1-2	open	1-2	2-3, 4-5	open	open	open	close	close
Cyrix 486 DX/DX2/DX4 [M7]	2-3	1-2	open	1-2	1-2, 4-5	open	close	close	open	open
Cyrix 486 DX4-100 [Intel SMM type]	2-3	1-2	close	1-2	1-2, 4-5	open	open	open	close	close
UMC 486 (U5S/U5SX)	1-2	2-3	open	2-3	open	close	open	open	open	open

Jumper Notes

- RN11 is always open on MB-8433UUD versions 2 & 3. RN11 needs to be closed for U5S and U5SX.
- AMD X5-133 and Cyrix 5x86-133 respond to the 2× multiplier setting by multiplying the FSB by 4× internally.
- AMD CPUs marked "A80486xxx-xxxNV8T" or "A80486xxx-xxxSV8T" only support write-through L1 cache
- AMD CPUs marked "A80486xxx-xxxSV8B" support write-back L1 cache
- Intel P24D CPUs marked "&EWxxxx" support write-back L1 cache
- Intel P24C CPUs marked "&Exxx-xxx" support "green" functions

PS/2 Mouse Pin Assignments

PS/2 Port (female)
(as the mouse connector sees it)



PS/2 Header (JP47)

Pin #	Assignment
1	Data (brown) - Routes to pin 199 of UM8886BF
2	N/C
3	Gnd (red)
4	Vcc (orange)
5	Clk (yellow) - Routes to pin 200 of UM8886BF

BIOS Settings

My default BIOS settings for 33/40 MHz FSB and 256 KB double-banked cache.

STANDARD CMOS:

Primary Master - None
Primary Slave - None
Secondary Master - None
Secondary Slave - None

Set to *Auto* if using an IDE hard disk, or *None* if using SCSI or a PCI ATA controller.

Drive A - 1.44M, 3.5 in.
Drive B - 1.2M, 5.25 in.
Video - EGA/VGA
Halt On - All Errors

BIOS FEATURES:

Virus Warning - Disabled
CPU Internal Cache - Enabled
External Cache - Enabled
Memory Parity Check – Disabled

This can be enabled if your RAM contains the parity chips, however if you soft-reboot, you will sometimes receive NMI parity errors and the system must be hard-reset.

Quick Power On Self Test - Enabled
Boot Sequence - A,C
Swap Floppy Drive - Disabled
Boot Up Floppy Seek - Disabled
Boot Up NumLock Status - On
Boot Up System Speed - High

Gate A20 Option - Fast

A20 refers to the first 64 KB of extended memory, also known as the high memory area. This option uses a faster way to access memory above 1 MB as opposed to the normal "keyboard controller" route.

Typematic Rate Setting - Disabled
Typematic Rate (Char/Sec) - 6
Typematic Delay (Msec) - 250
Security Option - Setup
Delay Before HDD Detection - Disabled
OS Select for DRAM > 64MB - Non-OS/2
PCI/VGA Palette Snoop - Disabled
IDE Second Channel Control - Enabled

Video BIOS Shadow - Enabled
C8000-CBFFF Shadow - Disabled
CC000-CFFFF Shadow - Disabled
D0000-D3FFF Shadow - Disabled
D4000-D7FFF Shadow - Disabled
D8000-DBFFF Shadow - Disabled
DC000-DFFFF Shadow - Disabled

CHIPSET FEATURES:

Auto Configuration - Disabled

L2 Cache Wait States - 2-1-1-1 (25-40 MHz FSB & 256 KB double-banked cache & FPM memory)
(if using 512 KB single-banked cache and 33 MHz FSB, 2-1-1-1 OK)
(if using 512 KB & 40 MHz+, slower wait states are required for stability)
3-2-2-2 is required for a 66 MHz FSB.

2-1-1-1 = 5 clock cycles
3-1-1-1 = 6 clock cycles
2-2-2-2 = 8 clock cycles
3-2-2-2 = 9 clock cycles

These are the clock cycles needed to read four 32-bit words by the CPU from L2 cache (cache read hit). The lead-off word read usually takes longer because it also has to decode the start address as well as read the data.

DRAM Read Wait States - 0 WS (25-40 MHz FSB)
Set to 1 WS if using a 66 MHz FSB and one stick of 64 MB FPM.
Set to 2 WS if using a 66 MHz FSB and two sticks of 64 MB FPM.

DRAM Write Wait States - 0 WS

EDO DRAM Install Option - Disabled
Enable *only* if you have EDO DRAM. FPM RAM seems to work best with a 66 MHz FSB.

Slow Refresh (1/4 Freq) - Enabled

L1 Cache Update Scheme - Wr-Back

L2 Cache Update Scheme - Write-Through or Write-Back
Depends on the amount of system memory. You do not want to exceed the cacheable range. Write-back works best if FSB = 66 MHz.

Alt Bit in Tag SRAM - 8 + 0
8 + 0 when using write-through L2 cache, or 7 + 1 if using write-back L2 cache.

Early Cache Write Mode - Enabled

Burst Copy-Back Option - Enabled

Host-to-PCI Post Write - 0 WS

Host-to-PCI Burst Write - Enabled

PCI Bus Park Option - Enabled

PCI Posted Memory Write – Enabled

Preempt PCI Master Option - Disabled

Key Controller Clock - 7.16 MHz or PCI/4

Host Clock / PCI Clock - 1:1
1:1 for 20, 25, 33 MHz FSBs; 1:1 will sometimes work with a 40 MHz FSB, but may require 1:2/3 for stability; 1:2/3 for a 50 MHz FSB; 1:1/2 for a 66 MHz FSB.

ISA Bus Clock Option - PCICLK/4

IBC DEVSEL# Decode - Slow
Medium also works. Fast may trash certain hard drives.

I/O Recovery Time - 2BCLK (set to 4BCLK if FSB=66 MHz)

System BIOS Cacheable - Enabled

Video BIOS Cacheable - Enabled

Onboard FDD Controller - Enabled

Onboard Parallel Mode - ECP

Onboard Parallel Port - 378H

Onboard Serial Port 1 - COM1/3F8

Onboard Serial Port 2 - COM2/2F8

PCI/GREEN FUNCTION:

PnP BIOS Auto-Config - Enabled

It is sometimes required to set this to *Disabled* if some of your ISA/PCI cards have IRQ sharing conflicts. In which case, it is best to set the available IRQ's to,

1st Available IRQ – 7	11 if 66 MHz FSB and Feipoa's hardware
2nd Available IRQ – 9	9 if 66 MHz FSB and Feipoa's hardware
3rd Available IRQ – 10	NA if 66 MHz FSB and Feipoa's hardware
4th Available IRQ – 11	NA if 66 MHz FSB and Feipoa's hardware

In general, the following PIC table applies.

0	System Timer
1	Keyboard Controller (i8042)
2	Slave from IRQ 9 - leave alone!
3	COM 2/COM 4
4	COM 1/COM 3
5	*General Use* (or Audio)
6	Floppy Controller
7	*General Use* (or LPT)
8	Real-Time Clock (RTC)
9	*General Use* (or VGA) - Redirected to IRQ 2
10	*General Use* (or USB)
11	*General Use* (or SCSI cards, Windows Sound)
12	PS/2 Mouse (i8042)
13	Math coprocessor
14	Primary IDE (or SCSI if Primary IDE disabled)
15	Secondary IDE (or SCSI if Secondary IDE disabled)

Slot 1 Using INT# - AUTO

Slot 2 Using INT# - AUTO

Slot 3 Using INT# - AUTO

PCI IRQ Activated By - Level

PCI IDE Controller - Enabled

PCI IDE IRQ Map To - PCI-Auto

Primary IDE INT# : A

Secondary IDE INT# : B

IDE HDD Block Mode - Enabled

IDE Primary Master PIO - Auto [CF cards do not boot properly when set to Auto. Set to PIO-4 when using CF cards]

IDE Primary Slave PIO - Auto

IDE Secondary Master PIO - Auto

IDE Secondary Slave PIO - Auto

Assign IRQ For VGA - Enabled

Enable if using Windows 95/98/ME (required for bus mastering). If using Windows NT4/2000, set to Disabled as Windows NT/2000 will assign an available IRQ. Alternately, you can leave this enabled for NT4/2000, but ensure that IRQ9 is available in Windows. If using an AWE64, for example, sometimes Windows assigns IRQ9 to the AWE64, in which case, use Control Panel to set the AWE64 (or any other card using IRQ9) to IRQ5/Basic Configuration before enabling this option in the BIOS.

IRQ3 Wake Up - Enabled

IRQ4 Wake Up - Disabled

IRQ5 Wake Up - Enabled

IRQ7 Wake Up - Disabled

IRQ9 Wake Up - Enabled

IRQ10 Wake Up - Enabled

IRQ11 Wake Up - Enabled

IRQ12 Wake Up - Enabled

IRQ14 Wake Up - Enabled

IRQ15 Wake Up - Disabled

POWER MANAGEMENT:

Power Management - User Define
PM Control By APM - Enabled
Video Off Method - DPMS Support
HDD Standby Timer - Disabled
Doze Timer Select - 16 Min
Standby Timer Select - 64 Min
Inactive Timer Select - 128 Min

Doze Mode - 1/2 HCLK, Display Turn On
Standby Mode - 1/4 HCLK, Display Turn Off
Inactive Mode - 1/8 HCLK

PCI Master3 Check - Enabled
PCI Master2 Check - Enabled
PCI Master1 Check - Enabled
VESA Slave Access Check - Disabled
LPT Access Check - Enabled
COM Access Check - Enabled
ISA Master & DMA Check - Enabled
IDE Access Check - Disabled
Floppy Access Check - Enabled
VGA Access Check - Enabled
I/O Region Access Check - 1F0h-1FFh